TÜBİTAK
MARMARA BİLİMSEL VE ENDÜSTRİYEL ARAŞTIRMA ENSTİTÜSÜ

ELEKTRONİK ARAŞTIRMA BÖLÜMÜ

DESIGN OF DIGITAL PHASE SHIFTERS SUITABLE FOR MONOLITHIC IMPLEMENTATION

B. S. YARMAN

January, 1984

Technical Report No : 1

GEBZE - KOCAELİ

MAE MATBAASI - GEBZE

TÜRKİYE BİLİMSEL VE TEKNİK ARAŞTIRMA KURUMU
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621.38.04(047.3)=20
YAR
1984

Yarman, (Binboğa) (Sıddık)
Design of digital phase shifters suitable for monolithic implementation. Gebze, MAE Mat., 1984.
pp., figs., 1 table, 4°.
TÜBİTAK Marmara Bilimsel ve Endüstriyel Araştırma Enstitüsü Elektronik Araştırma Bölümü. Technical Report No.1.
Konu: 1)Elektronik devreleri-dizaynı 2)Faz kaydırıcılar 3)Mikrodalga 4)Dalga hareketi teorisi

ABSTRACT

In this paper, primarily the diode switching circuits, conventional loaded line and reflection phase shifters are reviewed. The presentaiton is carried out in a theoretical manner rather than microwave engineering formulation. Secondorily, four novel digital phase shifter configurations which are suitable for monolithic fabrication are presented. Operation of the new circuits is based upon the phase shifting properties of symmetrical lowpass and highpass L-C ladders. In the new designs, use of ideal microwave switches, loaded lines, switched lines and hybrids are not required. Thus especially at extra high frequencies, significant losses due to these elements are eliminated. Theoretical analysis indicates that new phase shifter configurations provide improved phase shifting performance over the classical approaches.

Explicit design equations are presented for each phase shifter studied in this paper. Design examples are also included to emphasize the practical use of the new approaches.

I. INTRODUCTION

In the design of large antenna array systems, there is an increasing demand to design low-loss phase shifters, especially at extra high frequencies (EHF). Circuit losses are basically due to switching elements as well as mismatch and passive components. Switching losses are inevitable. However, passive component losses may be reduced by choosing the monolithic approach since it provides compact size.

In this study, first the diode switching circuits in digital phase shifters, and conventional loaded line and reflection phase shifters are presented. The presentation is carried out in a circuit theoretic approach rather then classical microwave engineering formulation. Then four novel digital phase shifter configurations which are suitable for monolithic implementation are introduced. It is shown that these circuit configurations provide better phase shifting performance over the loaded line and reflection phase shifter approaches.

II. DIODES AS SWITCHING ELEMENTS

In the design of digital phase shifters, PIN diodes may be used as switching elements. In this section, different diode switching circuits which can be used in the phase shifter design are studied.

A simple pin diode model is shown in figure 1a. In practice, the ideal behavior of the diode is perturbed by forward (R_f) and reverse (R_r) biased resistances which should be close to each other and as small as realizables at the switching states.

A diode may be used as a series switch as shown in figure 1b In the high frequency applications for practical realization, an inductance L in parallel with the diode is used to adjust diode capacitance C_D yielding the effective capacitor C at the center frequency f_o. The shunt inductance L is given by:

$$w_o L = \frac{1}{C_D - C} \qquad (1)$$

A shunt switch may be realized using a single diode as shown in Figure 2. When D is reverse biased, shunt inductance L_A and equivalent capacitor

$$C_T = \frac{C_A \cdot C_D}{C_A + C_D} \tag{2}$$

produces either a desired value of an effective inductance L or a capacitor C, or both. In the forward biase state of the diode, elements L_A and C_A resonate at the center frequency f_o ($W_o = 2\pi f_o = 1$, normalized). Thus, the shunt switch is open at this state.

The element values of the shunt switch to produce an inductance L for an effective capacitance C and for a given diode capacitor C_D can be approximated as follows:

$$C_A \cong \frac{C + \sqrt{C^2 + 4CC_D}}{2} \tag{3}$$

$$L_A \cong \frac{1}{C_A - C} \tag{4}$$

Another switch which consists of an inductance in series with a diode D can be used both in shunt and series configurations (Figure 3). When D is reverse biased:

(a) $Z(jw) = jw\,L_A + \frac{1}{jwC_D}$ may resonate at f_o and it acts as a short circuit at the design frequency f_o,

(b) $Z(jw_o)$ approximates a capacitor C

(c) $Z(jw_o)$ acts as an inductor L.

When diode D is forward biased, actual inductance L_A is seen across the switch terminals.

III LOADED LINE PHASE SHIFTERS

A transmission line with electrical length θ_o can be used, as a phase shifting unit if the line is symmetrically loaded with series or paralel reactive immitances at both ends (Figure 4) [1],[2] Let "A" (BIT-IN) and "B" (BIT-OUT) represent different switching states. At state A, the transmission line is loaded with reactive loads X_A (or suseptive load Y_A), otherwise X_B (or Y_B).

In Figure 4, the series loading X may be considered as a lossless two-port [X].

Let $(S_{xkl}) = (\rho_{xkl}\ e^{j\emptyset_{xkl}})$ (5)

and $(E_{kl}) = (\rho e_{kl} \cdot e^{j\emptyset_{ekl}})$ $k,l = 1,2$ (6)

be the scattering parameters of the load network [x] and the transmission line (θ_o) respectively using the losslessness condition of (θ_o) the scattering parameters E_{ij} can be obtained as:

$$E_{11} = E_{22} = 0 \tag{7}$$

$$E_{12} = E_{21} = 1.e^{j\theta_o} \tag{8}$$

Let $(S_{kl} = \rho_{kl}e^{j\theta_{kl}})$, k, 1= 1,2 denote the scattering parameters of the loaded line shown in figure 4.
Then, it can be shown that

$$S_{11} = S_{22} = j\ \frac{2X - X^2\mu}{2(1-\mu X) + j(2\mu + 2X - X^2\mu)} \tag{9}$$

where $\mu = \tan\theta_o$ (10)

The transfer scattering parameter S_{21} can be written as in [3]

$$S_{21} = \frac{S_{x21}^2 E_{21}}{1 - E_{21}S_{x11}} \tag{11}$$

For an ideal phase shifter, the transmission loss should be zero. Thus;

$$|S_{11}|^2 = |S_{22}|^2 = 1 - |S_{21}|^2 = 0 \tag{12}$$

and employing (9),

$$2X - X^2\mu = 0 \tag{13}$$

or

$$\mu = \tan \theta_o = \frac{2}{X} \tag{14}$$

On the other hand, desired phase shift $\Delta\emptyset$ is defined as the phase difference between $\emptyset_{21A}$ and $\emptyset_{21B}$. That is,

$$\Delta\emptyset = \pm(\emptyset_{21A} - \emptyset_{21B}) \tag{15}$$

where $\emptyset_{21A}$ and $\emptyset_{21B}$ are the corresponding phases of S_{21} at states A and B respectively.

For a given reactance X,

$$\emptyset_{21} = 2 \tan^{-1}(\frac{X}{2}) = \theta_o \tag{16}$$

Considering (15) together with (16), under perfect matched conditions

$$\Delta\emptyset = \pm 2 \left(\tan^{-1} \frac{X_B}{2} - \tan^{-1} \frac{X_A}{2}\right) \tag{17}$$

At this point, it is important to notice that under perfect transmission conditions (14) defines two different electrical lengths $\theta_{oA} = \tan^{-1} \frac{X_A}{2}$ and $\theta_{oB} = \tan^{-1} \frac{X_B}{2}$ for the transmission line θ_o which is not realizable. For small phase changes, however, the transmission loss at both states A and B can be neglected and θ_{oA} and θ_{oB} will be close to each other. In this case, (17) is safe to use and the length θ_o can be

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or

$$\mu = \tan \theta_o = \frac{2}{X} \qquad (14)$$

On the other hand, desired phase shift $\Delta\phi$ is defined as the phase difference between ϕ_{21A} and ϕ_{21B} . That is

$$\Delta\phi = \pm(\phi_{21A} - \phi_{21B}) \qquad (15)$$

where ϕ_{21A} and ϕ_{21B} are the corresponding phases of S_{21} at states A and B respectively.

For a given reactance X,

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chosen between θ_{oA} and θ_{oB} (or θ_{oB} and θ_{oA}) to minimize and balance the insertion loss at both states.

Our practical experience indicates that for $|\Delta\phi| \leq 45^{o}$ it may be convenient to choose θ_o as

$$\theta_o \cong \frac{\theta_{oA} + \theta_{oB}}{2} \tag{18}$$

or

$$\theta_o = \sqrt{\theta_{oA} \cdot \theta_{oB}} \tag{19}$$

Based upon the above analysis, it is concluded that, there is an inavitable mismatch loss build in the loaded line phase shifters since the center line θ_o can naver satisfy the perfect transmission condition of ('0) simultaneously if both X_A and X_B are differant from zero (or Y_A, $Y_B \neq \infty$)

Therefore, it is appropriate to name these phase shifters as "intrinsically mismatched" loaded line phase shifters.

For the large phase changes, one may wish to employ perfectly matched loaded line phase shifters at both states which are described in the following section.

PRACTICAL LOADED LINE PHASE SHIFTERS

A typical series loaded line configuration is shown in Figure 5a. The reactive impedances of diodes D_1 and D_2 are transformed on the center line over the transformers $[\theta_T]$. The desired phase shift $\Delta\phi$ is achieved when the diodes are swicthed on and off. Depending on the switching states of the diodes, series reactances X_A and X_B load the center line θ_o. For a given diode capacitance C_D and the phase shift $\pm\Delta\phi$, the line lengths θ_o and θ_T can easily be computed at the center frequency f_o.

Let us introduce the new parameters X_L β and μ_T as follows:

$$X_L = -\frac{1}{W_o C_D} = -\frac{1}{C_D} \text{ (at } W_o = 1) \tag{20}$$

$$\beta = \frac{1}{2} \tan\left(\frac{\Delta\phi}{2}\right) \tag{21}$$

$$\mu_T = \tan\theta_T \tag{22}$$

For small phase changes, (17) can be used to approximate β:

$$\beta = \frac{X_A - X_B}{4 + X_A X_B} \tag{23}$$

Employing transmission line equations [4] X_A and X_B are calculated :

$$X_A = \frac{4\beta + X_B}{1 - X_B} = \frac{X_L + X_B}{1 - X_B X_L} \tag{24}$$

$$X_B = \frac{3\beta X_L \pm \sqrt{\Delta_a}}{2(\beta - X_L)} \tag{25}$$

where $\Delta_a = 9\beta^2 X_L^2 - 4(4\beta - X_L)(\beta - X_L)$. Thus, the transformer length θ_T is found :

$$\theta_T = \tan^{-1} \mu_T \tag{26}$$
$$= \tan^{-1} X_B$$

Under the perfect transmission conditions, the line lengths

$\theta_{oA} = \tan^{-1} \frac{2}{X_A}$

and

$\theta_{oB} = \tan^{-1} \frac{2}{X_B}$ are calculated, and the center line length θ_o is chosen as

$$\theta_{o\,(A \text{ or } B)} \leqslant \theta_o \leqslant \theta_{o\,(B \text{ or } A)} \tag{27}$$

to minimize and equalize the transmission loss of the phase shifter at each switching state.

It should be noted that in (25) Δ_a should be non-negative ($\Delta_a \geq o$). If this is not the case, one must conclude that for given diode capacitance C_D, this particular phase shifter configuration cannot be used to obtaine the desired phase shift. However, effective value of the diode capacitance C_D may be reduced by shunting it with an inductance L_X.

Once the ideal element values of the phase shifter is calculated, detailed analysis, including the diode and other parasitics can be carried out using a computer program (e.g. ANA 5) Under many practical

circumstances, parallel loaded line phase shifters are more attractive to design engineers (Figure 5b) because of easy circuit realizations

Analysis of the parallel loaded line phase shifter with transformers θ_T is very similar to that of series one However, the same design equation can not be used by simply replacing reactance $jX_{(A \text{ or } B)}$ with suseptance $jY_{(A \text{ or } B)}$

When the diode D is forward biased, ideally, the load suseptance $Y_L = 1/Rf$ approaches to infinity and θ_T is calculated as follows

$$\tan \theta_T = \mu_T = - \frac{1}{Y_B} \tag{28}$$

Employing (28), Y_A and Y_B are calculated for the given phase shift $\Delta\emptyset$ as ;

$$Y_B = \frac{-3\beta \pm \sqrt{\Delta_b}}{2(1 + \beta Y_L)} \tag{29}$$

$$Y_A = \frac{Y_B Y_L - 1}{Y_B + Y_L} \tag{30}$$

where

$$\Delta_b = 9\beta^2 - 4(1 + \beta Y_L)(4\beta Y_L + 1)$$

and β is given by (21).

Employing (29-30), the line lengths θ_{oA} and θ_{oB} for perfect transmission are defined at the switching states A and B :

$$\theta_{oA} = \tan^{-1} \frac{2}{Y_A} + k\pi \tag{31}$$

$$\theta_{oB} = \tan^{-1} \frac{2}{Y_B} + k\pi \tag{32}$$

where k is set to 1 for $Y_{(A \text{ or } B)} < 0$, k=0 otherwise. Then the center line length θ_o is chosen as

$$\theta_o(\text{A or B}) \leq \theta_o \leq \theta_o(\text{B or A})$$

The phase shifters described above are suitable for small phase changes. On other hand, they suffer from poor tracking capability with high transmission loss, since there is an inevitable mismatch loss introduced at each switching state even if the ideal circuit elements are used in the design. In addition the effect of parasitics increase the transmission loss substantially as the operating frequency deviates from the center frequency f_o. Perfectly matched loaded line phase shifters, however, provide larger phase changes with improved transmission loss characteristics which in turn results in larger bandwidth

PERFECTLY MATCHED LOADED LINE PHASE SHIFTERS

A perfectly matched loaded line phase shifter with shunt loads is shown in figure 5c. In this figure, the center line θ_o is symmetrically loaded with the lumped switching circuits discussed in Section II (See Figure 3 also).

When D_1 and D_2 are reversed biased the shunt switches act as capacitor at the center frequency f_o.

In this case, the effective value of the loading capacitor C is given as a function of the phase shift $\Delta\emptyset$:

$$C = 2 \tan \left(\frac{\Delta\emptyset}{2}\right) \qquad (33a)$$

and the transmission line length θ_o is calculated using the perfect match condition of (14) :

$$\theta_o = 2 \tan^{-1} \left(\frac{2}{C}\right) \qquad (33b)$$

The tuning capacitor C_A and inductance L_A in the shunt switch are given by (4) and (5).

A simple version of a perfectly matched loaded line is shown in Fig. 5d [6] . In this circuit, when the diodes D are reverse biased, the center line θ_o is loaded by the reverse biase capacitance C. Under forward biase conditions, transmission line θ_o will be load free.

value of the load capacitance and the length of the line are calculated for perfect match conditions using (33).

Perfectly matched loaded line phase shifters certainly provide improved phase shifting performance over the mismatched lines as to larger bandwidth, smaller transmission loss, better tracking capability, etc. However, there are restrictive circumstances that may still call for lower loss and better tracking capability over a wide frequency band. Reflection type and the lumped element phase shifters, discussed throughout this paper, presumably offer better phase shifting performance over the loaded line phase shifters and they are also suitable for monolitic implementation.

REFLECTION PHASE SHIFTERS

Reflection phase shifters are widely used in practice due to their large phase shift capabilities. A phase shift of 180° can easily be accomplished without any difficulty [7]

Referring to figure 6a. when an incident wave "a" hits the lossless load (L), it will be completely reflected back with a certain amount of phase shift. At the load terminal plane, the phase shift between the incident wave "a" and the reflected wave "b" is given by the phase $\emptyset$ of the reflection coefficient S :

$$S = 1\, e^{j\emptyset} = \frac{Z_L - 1}{Z_L + 1} = \frac{1 - Y_L}{1 + Y_L} \qquad (34)$$

where $Z_L = jX_L$ represents the lossless load impedance, and $Y_L = 1/Z_L$ is the corresponding load admittance.

In order to make a physically realizable phase shifter, reflected wave "b" from the reactive termination should be received by a different port rather than input. Therefore, a simple reflection type time delay phase shifter must contain at least 3-port which is realized as a circulator. However, at high frequencies, physical implementation of the circulators become difficult. Instead, lossless 4-port circuits, are used with symmetric

reactive loading to design phase shifters. In any event, the phase change in a reflection phase shifter is determined by the phase change of the reflection coefficient of the reactive terminations. In figure 6b reflection phase shifters with shunt switching realized using branch-line couplers is shown. Element values of these switching circuits are easily adjusted to come up with the desired phase shift.

Reflection phase shifters offer some distinct advantages over the other phase shifters such as excellent phase tracking capability, wider bandwidth and idealy no mismatches at the input and output ports. On the other hand, the insertion loss of the phase shifter is highly sensitive to the element values when the losslessness of the switching circuits are perturbed by the practical implementations. In practice, loss of the 3-port or 4-port couplers which make the body of the phase shifter also contribute to the overall loss. This contribution, at the high frequencies, may not even be tolerable.

Therefore, at extra high frequencies (EHF) only large phase shifts (e.g 180^{o} shift) may be feasible to be realized using the reflection phase shifters. For small shifts, different approaches are preferred.

A 180^{o} BIT PHASE SHIFTER USING BRANCH LINE COUPLER WITH SHUNT SWITCH CIRCUITS:

In figure 6b, reactive loads act as inductances L when diodes are forward biased:

$$C_T - \frac{1}{L_A} = -\frac{1}{L}$$

or

$$L = \frac{L_A}{1 - C_T L_A} \qquad (35)$$

where

$$C_T = \frac{C_A \cdot C_D}{C_A + C_D}$$

When diodes D are reverse biased, shunt switches represent an effective capacitor C such that C=L.

On the other hand, C is also given as:

$$C = \frac{L_A C_A - 1}{L_A} \tag{36}$$

Employing (35-36) an expression for L_A is obtained:

$$(1 + C_A C_T)L_A^2 - (C_A + C_T)L_A + 1 = 0 \tag{37}$$

or $$L_A = \frac{(C_A+C_T) + \sqrt{(C_A-C_T)^2 - 4}}{2(1 + C_A + C_T)}$$

Notice that, in (37), choice of the tuning capacitor C_A can not be arbitrary, rather it should be chosen to yield a realizable value for L_A which can easily be obtained by examining the discriminator $\Delta_c > 0$ of (37)

$$\Delta_c = (C_A + C_T)^2 - 4(1 + C_A C_T) > 0$$

or

$$C_A - C_T > 2$$

Clearly, a minimum value for C_A is required to endup with a realizable L_A. Thus, for a given value of diode capacitance C_D, element values of the shunt switch is computed satisfying the realizibility condition of (59). The shunt inductance L_A is obtained by solving (37) Similar analysis can be carried out for different phase shifts.

3. Element L-C LADDERS AS PHASE SHIFTERS

In this section, we introduce four different digital phase shifter configurations based upon the operation of the lowpass and highpass, T and π section L-C ladders [8]. These circuits offer relatively better performance over the phase shifters discussed thorughout the paper. Furthermore, they are suitable for monolithic implementations.

Element vaules of a symmetric, 3-element lowpass or highpass ladder are chosen so that at a given frequency f_o, the ladder network yields the desired phase shift ϕ_s with zero insertion loss. Referring to Figure 7, let C and L be the normalized element values for capacitances and inductances respectively, and (S_{kl} (s); s = σ+ jw, k, l = 1,2) denote the unit normalized scattering parameters of the lossless ladders. On the jw axis,

$$S_{kl}(jw) = \rho_{kl}\, e^{j\emptyset kl}, \quad k, 1 = 1,2 \tag{39}$$

At the center frequency f_o, a desired phase shift $\emptyset_s$ with perfect transmission (i.e. zero insertion loss) is achieved when the following conditions are simultaneously satisfied:

$$\emptyset_s (W_o) = \emptyset_{21} (W_o) \tag{40a}$$

$$_{21}(W_o) = 1 \tag{40b}$$

Henceforth, all the derivations will be carried out to satisfy (40). Let us first compute the element values of high Pass T-section.

In Figure 7a, the input impedance $Z_{in}(s)$ of the highpass T is given by

$$Z_{in}(s) = \frac{LC^2S^3 + 2LCS + CS + 1}{LC^2S^3 + C^2S^2 + Cs} = \frac{N}{D}$$

$$= R(s^2) + \sigma(s) \tag{41}$$

where $R(s^2)$ and $O(s)$ are the even and odd part of $Z_{in}(s)$ respectively. In particular, the even part $R(s^2)$ is given as follows:

$$R(s^2) = \frac{A(s)\ A(-s)}{D\ D_*} \tag{42a}$$

where A(s) may be chosen as $A = -LC^2s^3$ (42b)

Employing the formulas given in [3], the transfer scattering coefficient S_{21} is obtained as

$$S = \frac{2A*}{N+D} \tag{43}$$

on the jw axis,

$$S_{21}(jw) = \rho_{21}\, e^{j\emptyset_{21}}$$

where

$$\rho_{21}^2 = \frac{4L^2C^4W^6}{(2CW - 2LC^2W^3)^2 + (1 - (2LC + C^2)W^2)^2}$$

and

$$\phi_{21}(w) = \frac{\pi}{2} - \tan^{-1}\left[\frac{2CW - 2LC^2W^3}{1 - (2LC+C^2)W^2}\right] \qquad (44)$$

After some manipulations, perfect transmission condition (40b) yields

$$W_o^2 = \frac{1}{2LC - C^2} \qquad (45)$$

Let us introduce a phase shift dependent parameter η

$$\eta = \tan\left[\frac{\pi}{2} - \phi_{21}(W_o)\right] \qquad (46)$$

Then, the phase condition 40a yields

$$\eta = \frac{2CW_o - 2LC^2W_o^3}{1 - (2LC+C^2)W_o} \qquad (47)$$

Fixing the normalized frequency $W_o = 1$, simultaneous solution of (45) and (47) yield the desired values for C and L:

$$C = \eta + \sqrt{\eta^2 + 1} \qquad (48)$$

$$L = \frac{1 + C^2}{2C} \qquad (49)$$

Similarly, for a high pass π-section (Figure 7 b);

$$L = \eta + \sqrt{\eta^2 + 1}, \qquad C = \frac{1 + L^2}{2L} \qquad (50)$$

For a low pass T-Section (Figure 7c);

$$L = \frac{1}{\eta + \sqrt{\eta^2 + 1}}, \qquad C = \frac{2L}{1 + L^2} \qquad (51)$$

For a low pass π-section (Figure 7d);

$$C = \frac{1}{\eta + \sqrt{\eta + 1}} \quad , \quad L = \frac{2C}{1 + C^2} \tag{52}$$

It should be noted that phase shifts between o^o and 180^o are possible with any of these low/high pass T or π Section L-C ladders (i.e. $0^o < \phi_s < 180^o$).

HIGH/LOW PASS BASED T AND π SECTION DIGITAL PHASE SHIFTER CONFIGURATIONS

In Figure 8a, a "high-pass-based" T-section digital phase shifter configuration is proposed. The diodes D_1, D_2 are identical and my be planar pin diodes in series configuraiton. The diode D_3 may have identical electric and physical characteristics as D_1 and D_2 and it could be a planar or mesa pin diode in shunt configuration.

When diodes D_1, D_2 and D_3 are reverse biased, they act as capacitors (C_D) with a small series reverse resistance R_r (Figure 8b) In this state, the desired phase shift ϕ is achieved with no transmission loss at the center frequency f_o of the passband by choosing an appropriate value for C_D

When diodes D_1, D_2 and D_3 are forward biased they act as closed switches with a small series resistance R_f (Figure 8c), and in the shunt branch, inductance L_A resonates with the capacitor C_A providing a perfect transmission for the RF input signals. Thus, the high-pass-based, T-section digital phase shifter is perfectly matched at the center frequency f_o for both (BIT-IN and BIT-OUT) states. However, small losses due to practical realization of the circuit elements are inevitable.

Design equations for the proposed phase shifter can be derived from equations (46), (47), (48 and (49)

$$C_A = \frac{1 + \sqrt{1 + 4C_D L}}{2L} \quad , \quad L_A = \frac{1}{C_A} \tag{53}$$

The element values C_D, C_A and L_A are all normalized with respect to center frequency f_o and R_o which is specified as the normalization number (generally $R_o = 50\Omega$).

A high pass based π-Section digital phase shifter circuit is suggested in Figure 9 . Here, the physical operation is similar to that of high pass T-Section. However, the element distribution of the π-Section phase shifter is, of course, different. The element values of this circuit are computed employing (50) and (53).

A low-pass-based T-section digital phase shifter configuration is introduced in Figure 10a. In this figure, when the identical diodes D are forward biased, in the series arms, only inductors L given by (51) will be seen. In the shunt branch, capacitance C_A together with inductance L_A act as an effective capacitor C which is also specified by (51). Thus, the operation of low-pass T is realized (Figure 10b.). When the diodes are reverse biased (Figure 10c) diode capacitors C_D are chosen to resonate with series inductance L. That is,

$$C_D = \frac{1}{L} \tag{54}$$

The shunt branch inductance L_A also resonates with the equivalent capacitor

$$C_T = \frac{C_A \cdot C_D}{C_A + C_D} \quad \text{at } f_o.$$

Thus, the input signal is transmitted to the output without interruption. In this case, C_A and L_A are given as follows :

$$C_A = \frac{C + \sqrt{C^2 + 4CC_D}}{2} \tag{55}$$

$$L_A = \frac{1}{C_A - C} \tag{56}$$

Finally, a low-pass-based π-section digital phase shifter is shown in Figure 11 . The physical operation of this phase shifter is similar to that of the low pass T-section. However, the effective values of C and

L in this case are given by (51) and (52) and C_D, C_A and L_A are also specified by (54), (55), and (56) respectively.

Each phase shifter configuration presented in this section have different element value distribution. Therefore, they find proper application for designing phasors at various frequency bands. They are also suitable for monolithic implementation since the body of the phase shifters are constructed using essentially all solid-state diodes. Furthermore, since the new configurations consist of lumped elements and are perfectly matched, they offer relatively better phase shifting characteristics (lower insertion loss, better phase tracking capability) over the conventional phase shifter circuits.

EXAMPLES

In this section, we will exhibit the application of the explicit formulas to design various phase shifters. Throughout the examples, simple diode circuit models as shown in Figure 1 are used with the element values supported by the measurements on the RCA-made silicon PIN diodes [8], [9]. Our measurements under different bias conditions are summarized in Table I.

DESIGN OF 45° -BIT PHASORS AT 44 GHz

A) Intrinsically mismatched parallel loaded line phase shifter (Figure 5b)

Given : $|\Delta\phi| = 45^\circ$, $f_o = 44$ GHz, $\hat{C}_D = 0.173$ pF (chosen from Table : I), $R_o = 50\Omega$, (50Ω system is assumed).

Unknowns : θ_o, θ_T

Computation steps:

1. $Y_L = W_o R_o \hat{C}_D = 2.418$

2. $\beta = 1/2 \tan (\pm \frac{\Delta\theta}{2})$, choose "+" sign $\beta = 0.209$

3. $A = 1 + \beta Y_L \cong 1.5$, $B = 3\beta \cong 0.621$, $C = 4\beta Y_L + 1 \cong 3.$

4. $\Delta_b = B^2 - 4AC \cong -17.6 < 0$. Since Δ_b should be positive, we return to step 2 and try $\Delta\phi = -45^o$. Thus, $\beta = 0.027$, $A = 0.499$, $B = -0.621$, $C \cong -1.003$ and $\Delta_b = 2.38967 > 0$

5. $Y_B = \dfrac{-B + \sqrt{\Delta_b}}{2A} = 2.17$, $\quad Y_A = \dfrac{Y_B Y_L - 1}{Y_B + Y_L} = 0.926$

6. $\theta_{OA} = \tan^{-1}\left(\dfrac{2}{Y_A}\right) = 65.15$, $\quad \theta_{OB} = \tan^{-1}\left(\dfrac{2}{Y_B}\right) = 42.65^o$
(k=0 is chosen)

7. $\theta_{oA} < \theta_o < \theta_{oB} \quad \theta_o = 53^o$.

8. $\theta_T = \tan^{-1}\left(-\dfrac{1}{Y_B}\right) + 180$ or θ_T 155.2 (k = 1 chosen)

The performance of the above mentioned circuit was analyzed using our inhouse program ANA over the frequency band 43 GHz$<\Delta_f<$ 45 GHz. In the computations the diode losses were included as $R_f = R_r = 0.5\Omega$ and transmission line losses = 0.215 dB/cm was chosen. The line lengths θ_o and θ_T were adjusted to minimize the insertion loss over the passband. It was found that choice of $\theta_o = 45^o$, $\theta_T = 152^o$ yields improved performance over the previous design and it is summarized as follows:

Insertion loss: IL (dB);

$-0.71 <$ IL(dB) < -0.66: Diodes reverse biased.

$-1.34 <$ IL(dB) < -0.81 diodes forward biased

Phase shift; $|\Delta\phi|$

$36.1 < |\Delta\phi| < 58.7$ or, $|\Delta\phi| = 47^o \pm 11.3^o$ with $|\Delta\phi| = 45^o$ at $f_o = 44$ GHz

It should be noted that despite the final adjustements on the element values, intrinsically mismatched loaded line phase shifter configuration results in a poor phase tracking performance over the passband which may not be acceptable for some applications.

B) Perfectly-matched parallel loaded line phase shifter (Figure 5c)

Given : $\Delta\emptyset = 45^{\circ}$, $f_o = 44$ GHz, $\hat{C}_D = 0.173$ pF, $R_o = 50$

Unknowns : $\hat{L}_A$, $\hat{C}_A$, θ_o

Computation steps:

1. $C = 2 \tan\left(\frac{\Delta\emptyset}{2}\right) = 0.828$

2. $\theta_o = \tan^{-1}\left(\frac{2}{C}\right) = 67.5^{\circ}$

3. $C_D = W_o \hat{C}_D R_o = 2.418$

$$C_A = \frac{C + \sqrt{C^2 + 4CC_D}}{2} = 1.89$$

4. $$L_A = \frac{1}{C_A - C} = 0.943$$

5. $$\hat{L}_A = \frac{L_A}{W_o} R_o = 0.168 \text{ nH}, \quad C_A = \frac{C_A}{W_o R_o} = 0.135 \text{ pF}$$

Note that, the inductance value $\hat{L}_A = 0.168$ nH may not be realized as a lump circuit element. However, it may be replaced by an open or RF short shunt stub transmission line.

Assuming $R_r = R_f = 0.5\,\Omega$ and also including a series resistance $R_c = 0.5\,\Omega$ as the loss of C_A, the phase shifting performance of this phase shifter was analyzed over the frequency band 43 GHz $\leqslant f \leqslant$ 45 GHz. Phase tracking capability of this circuit is summarized as follows:

Insertion loss IL (dB)

$-0.808 \leqslant$ IL(dB) $\leqslant -0.757$; Diodes are forward biased,

$-0.385 \leqslant$ IL(dB) $\leqslant -0.378$; Diodes are reverse biased, and the phase change $|\Delta\emptyset|$ is,

$$43 < |\Delta\phi| < 46.5 \quad \text{with} \quad |\Delta\phi| = 45^{\circ} \text{ at } f_o = 44 \text{ GHz}$$

It is seen that perfectly matched parallel loaded line phase shifter provides a better phase shifting performance over the intrinsically mismatched loaded line. On the other hand intrinsically mismatched loaded line phase shifter offers more equalized insertion loss at different switching states. However, loss performance of the perfectly matched loaded line may be balanced and improved by choosing a proper value for the diode capacitance $\hat{C}_D$ and shunting it by an inductance.

C) Perfectly-matched low-pass-based T-section phase shifter :

Referring to Figure 8a let us calculate the element values of this phase shifter:

Given : $|\Delta\phi| = 45^{\circ}$, $f_o = 44$ GHz, $R_o = 50\Omega$

Unknowns : $\hat{C}_D$, $\hat{L}_A$, $\hat{C}_A$

Computation steps :

1. $\eta = \tan(90^{\circ} - 45^{\circ}) = 1$

2. $L = \dfrac{1}{\eta + \sqrt{\eta^2 + 1}} \cong 0.414, \qquad C_D \cong \dfrac{1}{L} = 2.41$

3. $C = \dfrac{2L}{1 + L^2} = 0.707,$

4. $C_A = \dfrac{C + \sqrt{C^2 + 4CC_D}}{2} \approx 1.707$

5. $L_A = \dfrac{1}{C_A - C} = 1$

6. $\hat{C} = \dfrac{C_D}{W_o R_o} = 0.173 \text{ pF}, \quad \hat{C} = \dfrac{C_A}{W_o R_o} = 0.122 \text{ pF}$

$$\hat{L} = \frac{1}{W_o} R_o = 0.074 nH$$

D) Perfectly matched lowpass-based π-Section phase shifter:

Given : $|\Delta\phi| = 45^o$, $f_o = 44$ GHz, $R_o = 50\Omega$

Unknowns : $\hat{C}_D$, $\hat{L}_A$, $\hat{C}_A$

Computation steps :

1. $\eta = \tan (90^o - 45^o) = 1$

2. $C = \dfrac{1}{\eta + \sqrt{\eta^2 + 1}} = 0.414$

3. $L = \dfrac{2C}{1 + C^2} = 0.707$, $C_D = \dfrac{1}{L} = 1.41$

4. $C_A = \dfrac{C + \sqrt{C^2 + 4CC_D}}{2} = 1$

5. $L_A = \dfrac{1}{C_A - C} = 1.707$

6. $\hat{C}_D = \dfrac{C_D}{W_o R_o} = 0.101$ pF, $\hat{C}_A = \dfrac{C_A}{W_o R_o} = 0.0175$ pF,

$L_A = \dfrac{L_A}{W_o} R_o = 0.305$ nH, $\hat{L} = \dfrac{L}{W_o} = R_o = 0.126$ nH

It is interesting to observe that the element value distribution of the π-section different from that of T-section. Similar results would be obtained by designing highpass based T/π section phosors. Different combinations of elements for various sections may be utilized successfully for designing multi-bit phase shifters at different frequencies.

We also designed 45^o - bit highpass-based T/π section phasors at the same center frequency and analyzed the phase shifting performance

of all the T/Π sections over 43 GHz $\leq \Delta f \leq$ 45 GHz. It was observed that they all yield similar phase shift porformances. Let us summarize the performance of the lowpass-based T-section including the diode losses ($R_f = R_r = 0.5\,\Omega$) and the loss associated with capacitor C_A ($R_C = 0.5\Omega$).

Passband : 43 GHz $\leq \Delta f \leq$ 45 GHz

Insertion loss (IL(dB)) :

$-0.22 \leq$ IL (dB) ≤ -0.211; Diodes are forward biased,

$-0.14 \leq$ IL (dB) ≤ -0.138; Diodes are reverse biased, and the phase shift $\Delta\emptyset$ is given as follows :

$$43 \leq \Delta\emptyset \leq 47 \quad \text{with} \quad \Delta\emptyset = 45^{o} \quad \text{at} \quad f_o = 44 \text{ GHz}$$

As it is seen throughout the examples, high/low pass-based T/Π section phase shifters yield superior phase tracking capability over the loaded line phase shifters. Furthermore, they are suitable for monolithic implementation.

CONCLUSION

In this paper first diode switching circuits, conventional loaded line and and reflection phase shifters have been reviewed from the circuit theory point of view rather than microwave engineering approach. Then, four novel digital phase shifter configurations are presented. In the new circuits, use of ideal microwave switches (S PDT, DPDT, etc.) transmission lines and 3 or 4-port couplers are not required. Thus especially at the extra high frequencies significant losses due to these elements are eliminated.

Similarities between the new topologies and highpass to lowpass lumped element phase shifters (10), (11) may be found. However in the new circuits numser of diodes and passive components are reduced since the switching state from highpass to lowpass is

eliminated. New phase shifters are also suitable for monolitic implementation since the body of the phase shifters are constructed usirg essentially all solid-state diodes. Initial computations indicate that new designs offer excellent phase tracking capability over the conventional approaches. Based upon the technology presented in (8), (9), it is anticipated that new phase shifter configuraitons will find applications for designing low loss monolitic PIN diode phase shifters with potential use at millimeter waves.

ACKNOWLEDGEMENT

Useful discussions with Mr. A. Rosen, Dr. W.R. Curtice, Mr. P. Stabile, Dr. H. Huang and Mr. A. Schwarzmann of RCA Corp, U.S.A and Dr. F.Y. Vural and Miss D. Balkan of Marmara Research Institute of Turkey are greatfuly acknowledged.

This work was completed at RCA Microwave Technology center, Princeton, N.J and supponsored by Electronic System Division Airforce Systems command, Hanscom Airforce Base MA, U.S.A under the contract F 19628-83-C-008.

REFERENCES

1. J.F.White, "Microwave Semiconductor Engineering", Reading, Van Nostard Reinhold Company, NY, 1982.

2. R.V. Garver, "Microwave Diode Control", Artech House, Inc. Dedham, Mass. 1976..

3. H.J. Carlin, B.S. Yarman, "The Double Matching Problem:Analytic and Real Frequency Solutions", IEEE CAS, Vol. 1, 1983.

4. S. Ramo, J.R. Whinnery and T. Van Duzer, "Field and Waves in Communication Electronics, "Reading, Wiley, 1965, NY.

5. S.M. Perlow, "ANA - Radio-Frequency Circuit Simulation and Analysis"- RCA Engineer, 27-6, Nov./Dec. 1982.

6. A. Schwarzmann, Private Communication.

7. A. Rosen, R.V. Martinelli, A.SChwarzmann, G.J. Brucker, G.H. Swartz, "High Power, Low Loss PIN Diodes for phased-array radar", RCA Review, Vol. 40, pp. 22, March 1979.

8. A. Rosen, M. Caulton, P. Stabile, A. Gombar, W.Janton, C. WU, J. Corboy, C. Magee, "Silicon as a Millimeter-Wave Monolithically Integrated Substrate A NEw Look", RCA REview, Vol. 42, December 1981, pp. 633.

9. Rosen et al, "Millimeter Wave Device Technology", IEEE, MIT, Vol.30, No. 1, January 1982.

10. P. Onno, A. Plilkins, "Miniature Multi KW PIN Diode MIC Digital Phase", IEEE G-MIT, IMSD CAT No. 71, pp. 22-23, 1971.

11. R.V. Garver, "Broadband Diode Phase Shifter", IEEE G-MTT, Vol.20, pp. 314-323, 1972

FIGURE CAPTIONS

FIGURE 1a: Simple pin diode model.

FIGURE 1b: Adjustments on the diode capacitance by means of a short inductance.

FIGURE 2 : A single diode shunt switch circuit.

FIGURE 3 : A single diode series switch circuit.

FIGURE 4 : Classical loaded line phase shifters.

FIGURE 5a: Intrinsically mismatched series loaded line phase shifter.

FIGURE 5b: Intrinsically mismatched parallel loaded line phase shifter.

FIGURE 5c: Perfectly matched series loaded line phase shifter.

FIGURE 5d: Perfectly matched parallel loaded line phase shifter.

FIGURE 6a: Reflection from a lossless load.

FIGURE 6b: Reflection phase shifter using branch line coupler with parallel switching circuit.

FIGURE 7a: Highpass T-Section

FIGURE 7b: Highpass Π-Section

FIGURE 7c: Lowpass T-Section

FIGURE 7d: Lowpass Π-Section

FIGURE 8a: Highpass based T-Section Digital Phase Shifter.

FIGURE 8b: Diodes are reverse biased.

FIGURE 8c: Diodes are forward biased.

FIGURE 9 : Highpass Based Π-Section Digital Phase Shifter.

FIGURE 10a: Lowpass Based T-Section Digital Phase Shifter.

FIGURE 10b: Diodes are reverse biased.

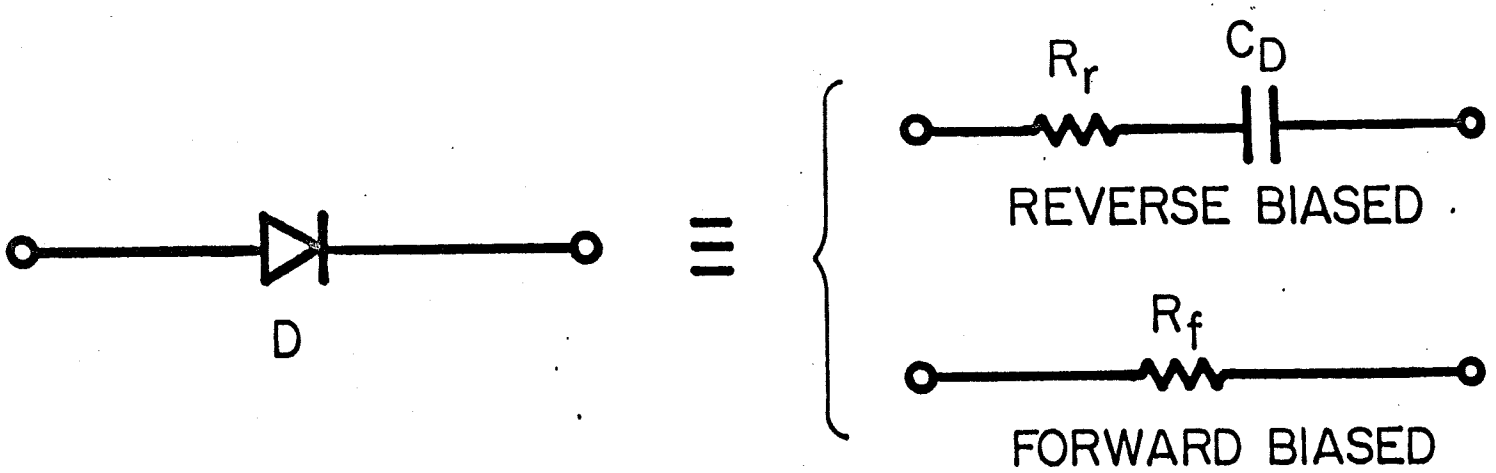
FIGURE 10c: Diodes are forward biased.

FIGURE 11 : Lowpass based Π-Section Digital Phase Shifter.

TABLE I

PIN DIODE MEASUREMENTS

FORWARD BIAS			REVERSE BIAS	
I(mA)	θ_D	R_f( )	V_R(V)	C(pf)
20	68	1.16	0	0.609
50	76	0.778	2	0.283
100	81	0.578	4	0.235
198	85	0.435	10	0.199
251	86	0.401	20	0.176
			40	0.173
			80	0.168
			150	0.167



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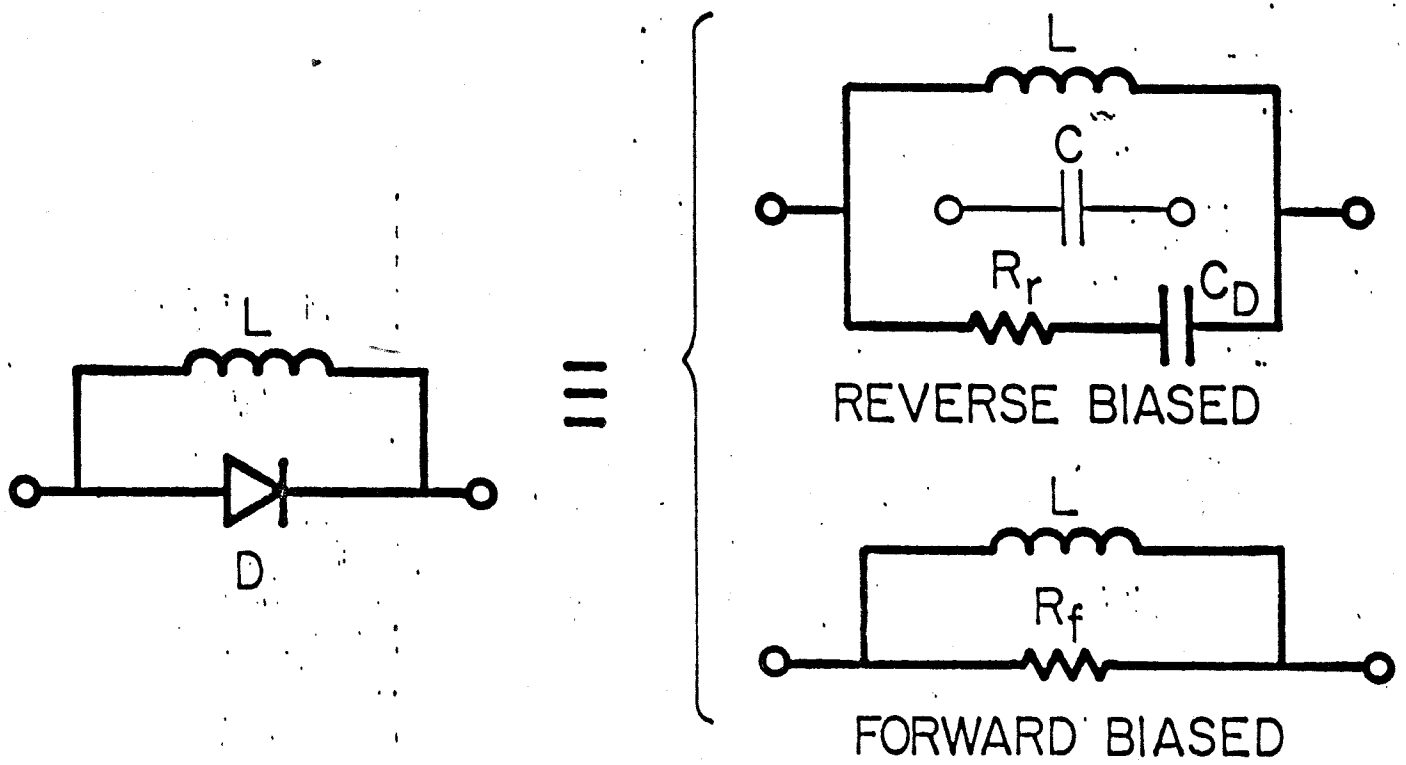

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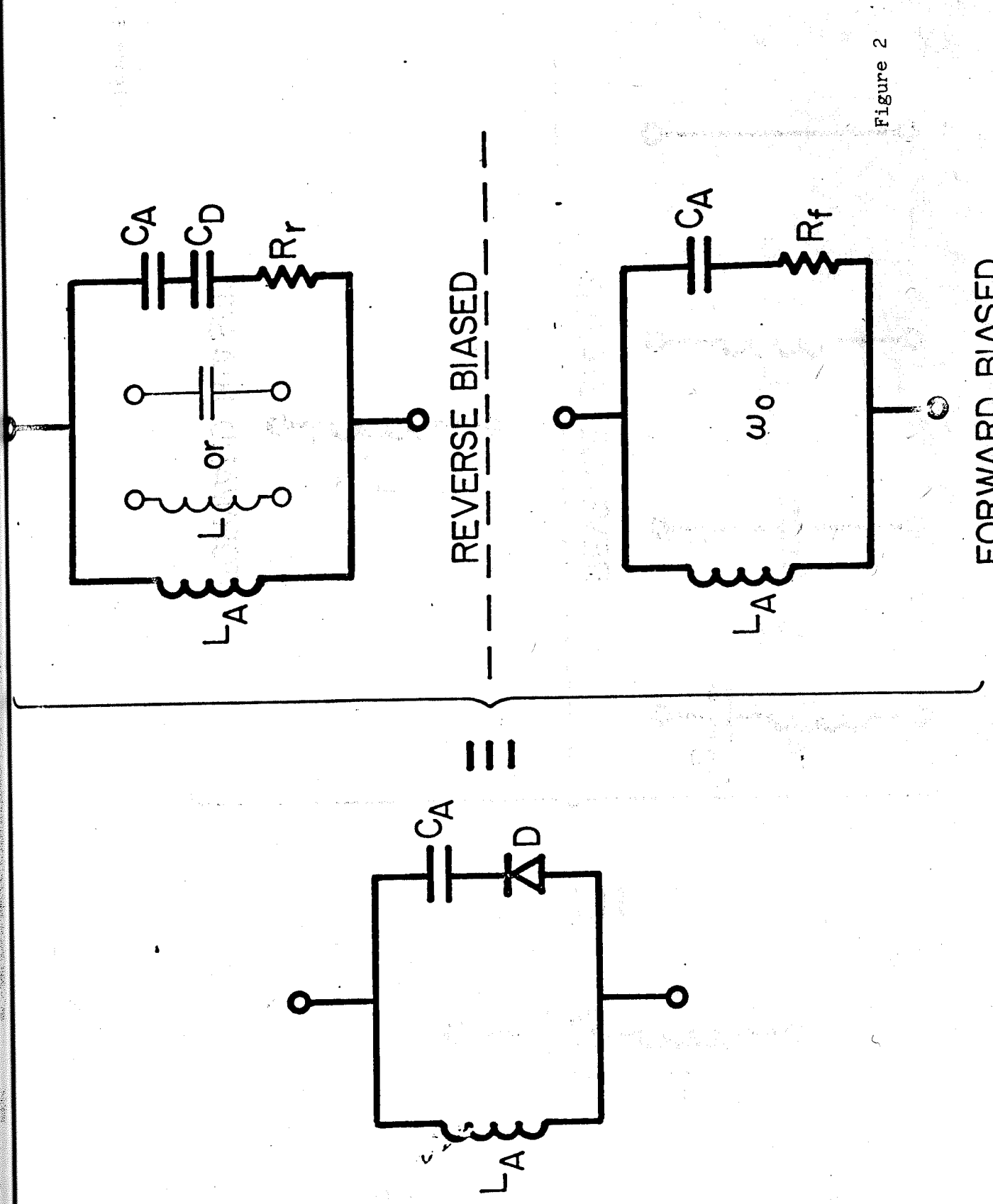
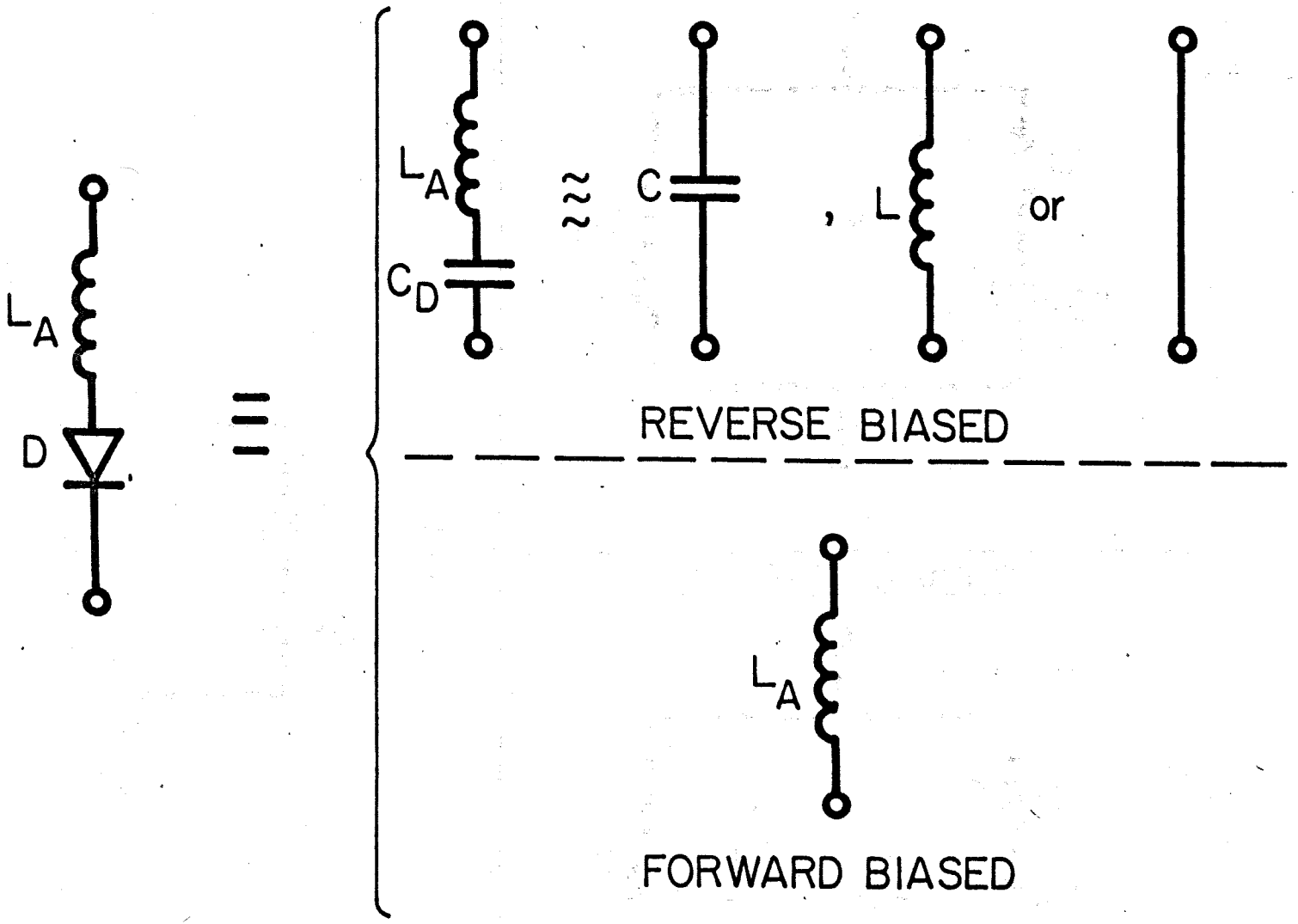

REVERSE BIASED
FORWARD BIASED
C_A
C_D
R_r
or
L
L_A
C_A
R_f
ω_o
L_A
=
C_A
D
L_A

Figure 2



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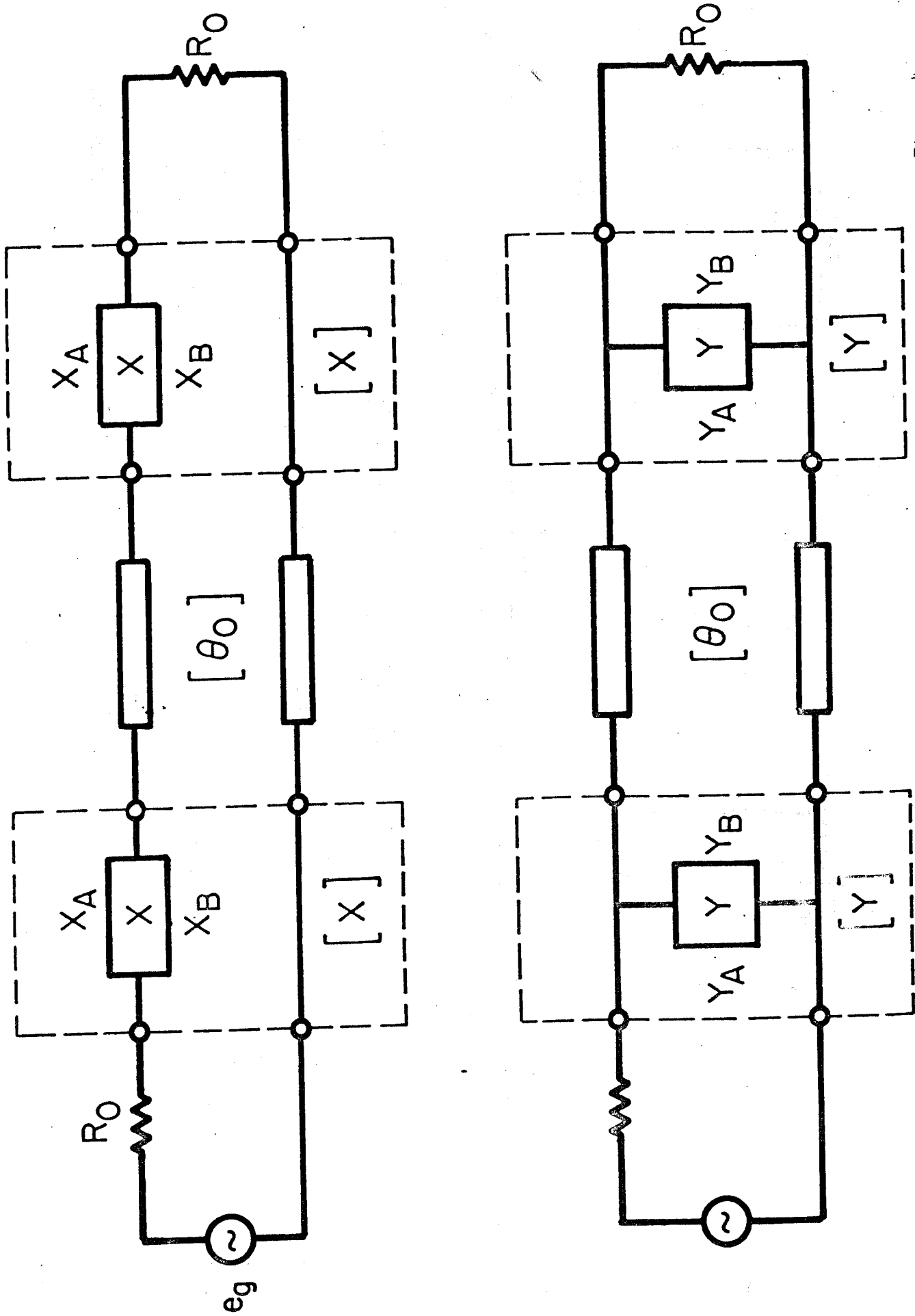

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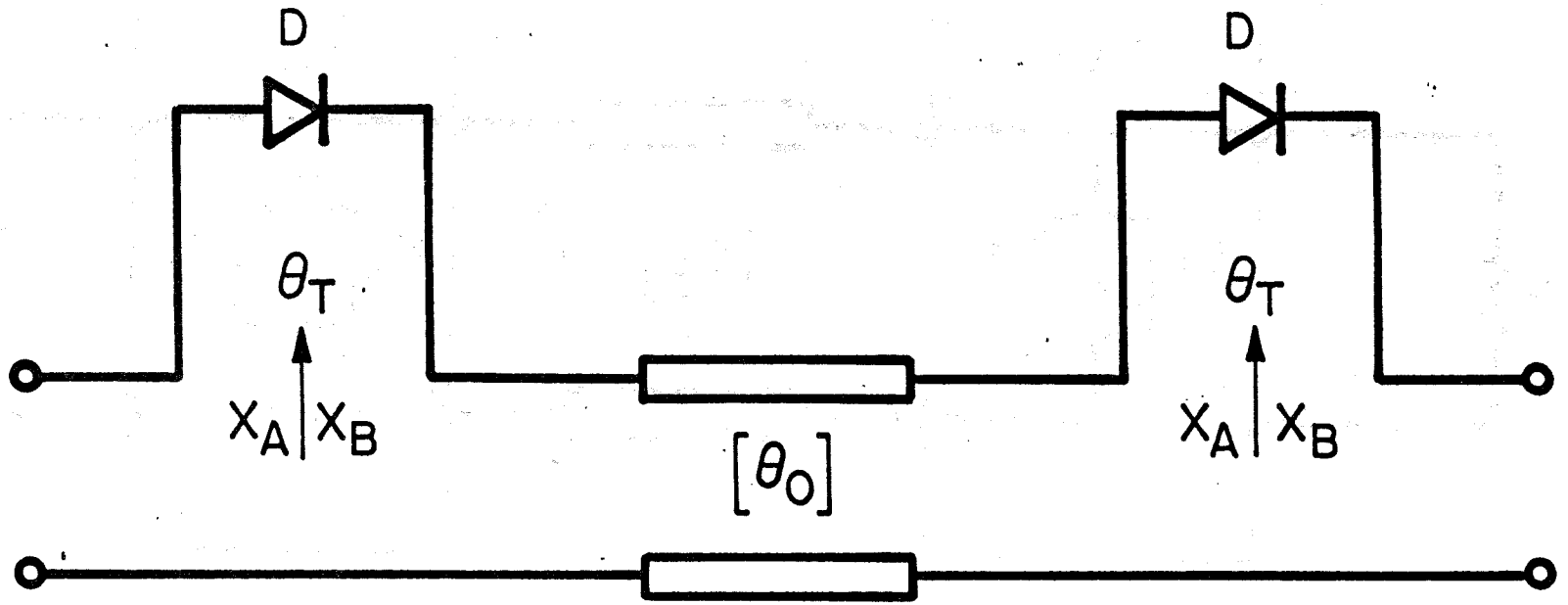
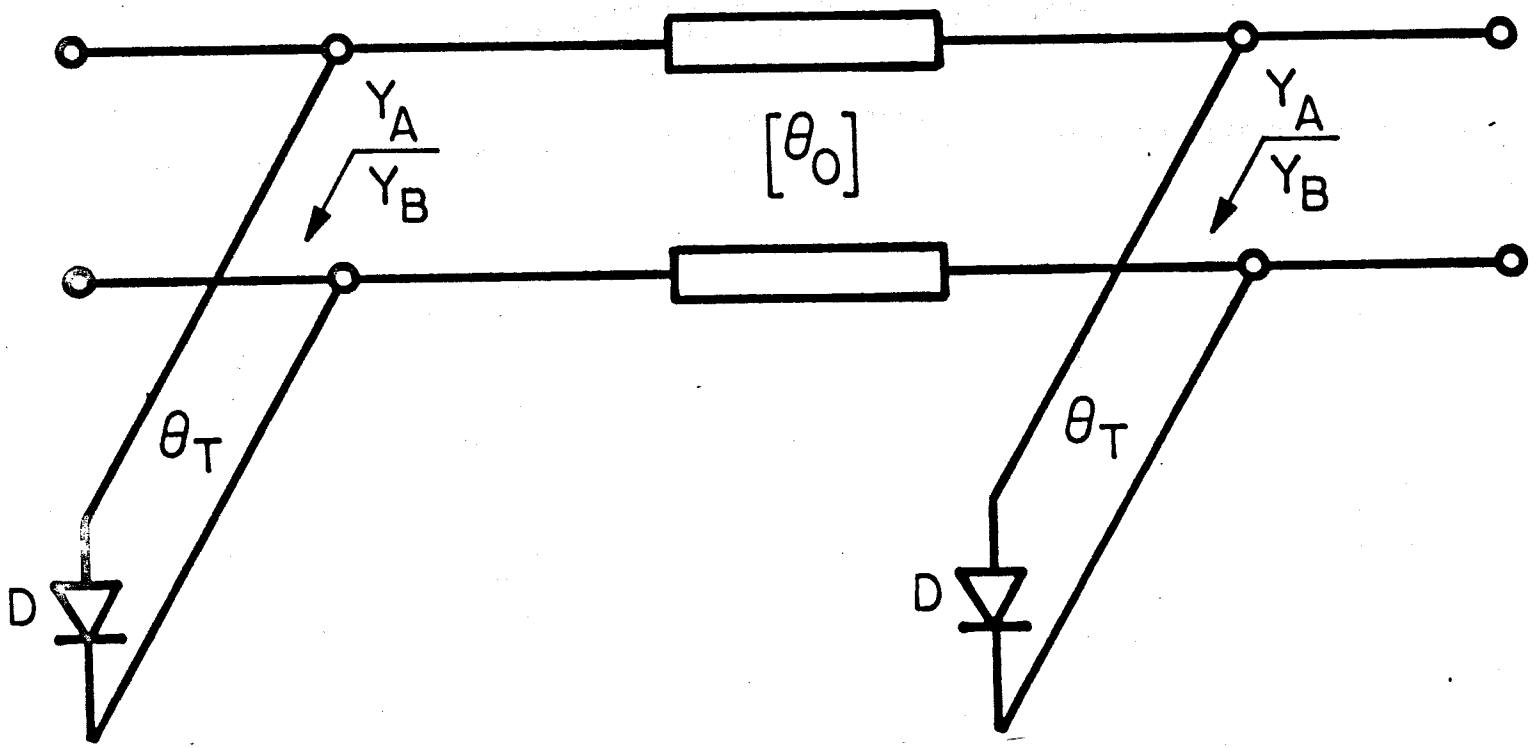


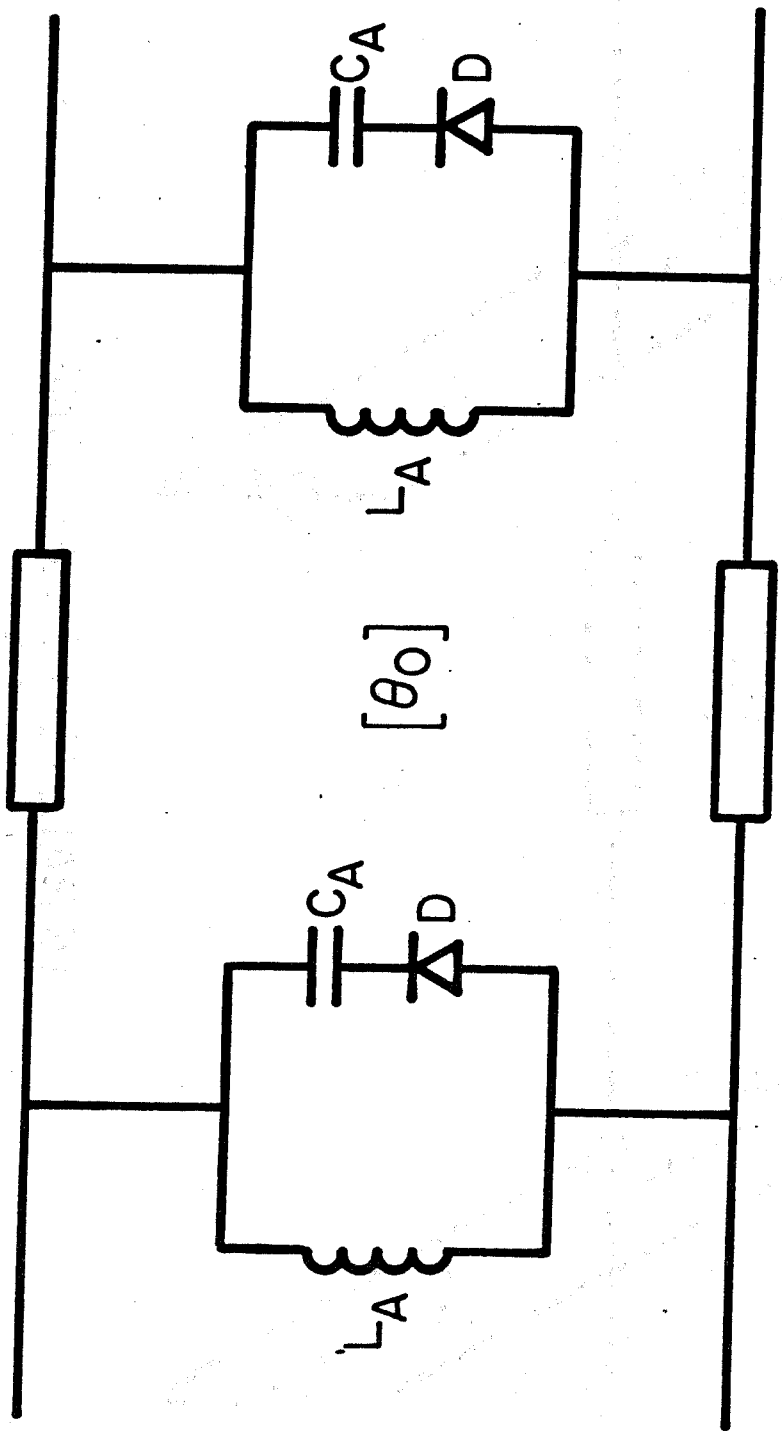
SERIES LOADED LINE
WITH
TRANSFORMER θ_T

Figure 5a



PARALLEL LOADED LINE
WITH
TRANSFORMERS θ_T

Figure 5b



PARALLEL LOADED LINE

Figure 5c

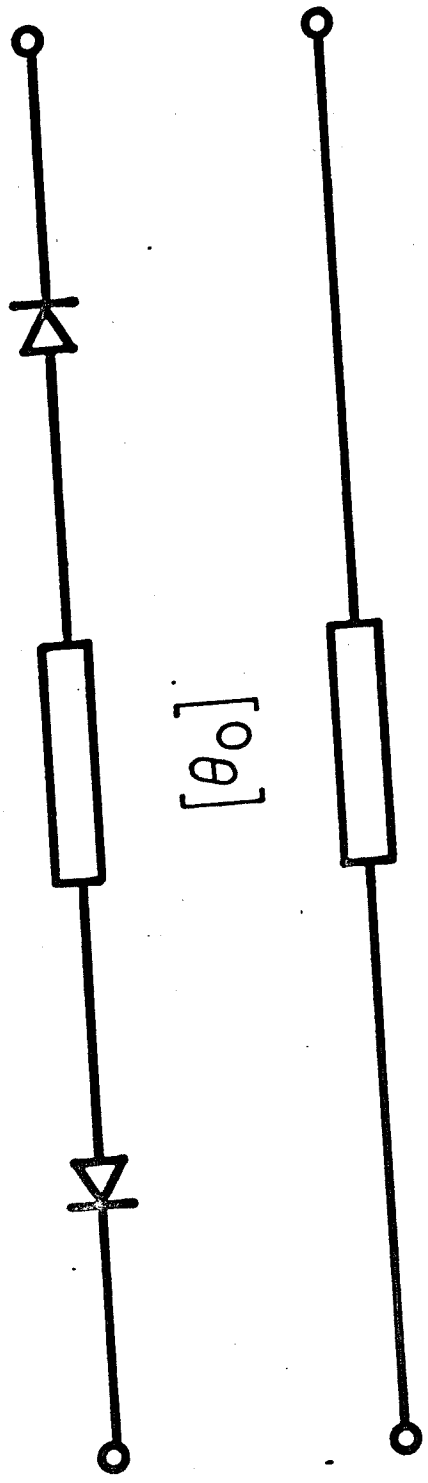
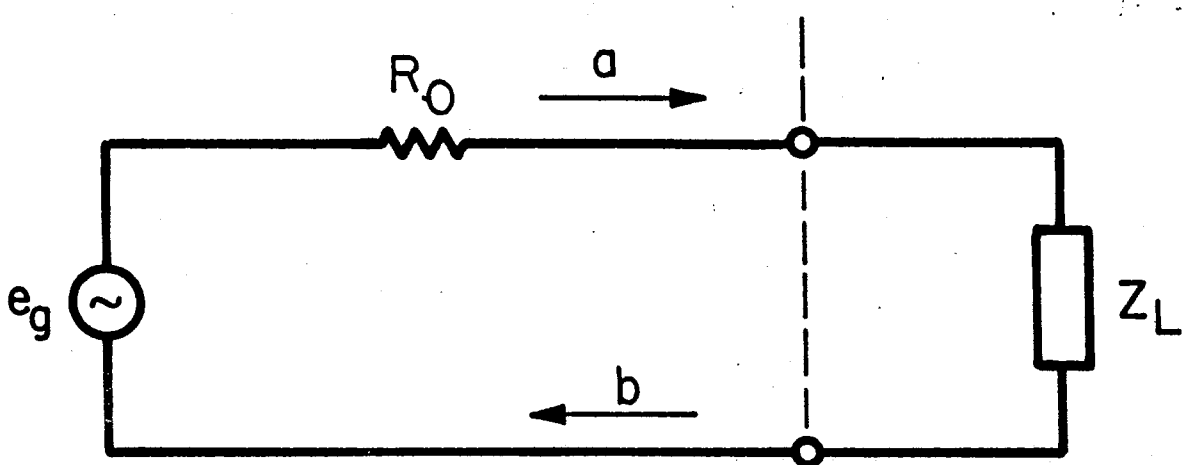


Figure 5d



$$S = \frac{1-Z_L}{1+Z_L}$$

$$= 1.e^{j\phi_L}$$

REFLECTION FROM A LOAD

Figure 6a

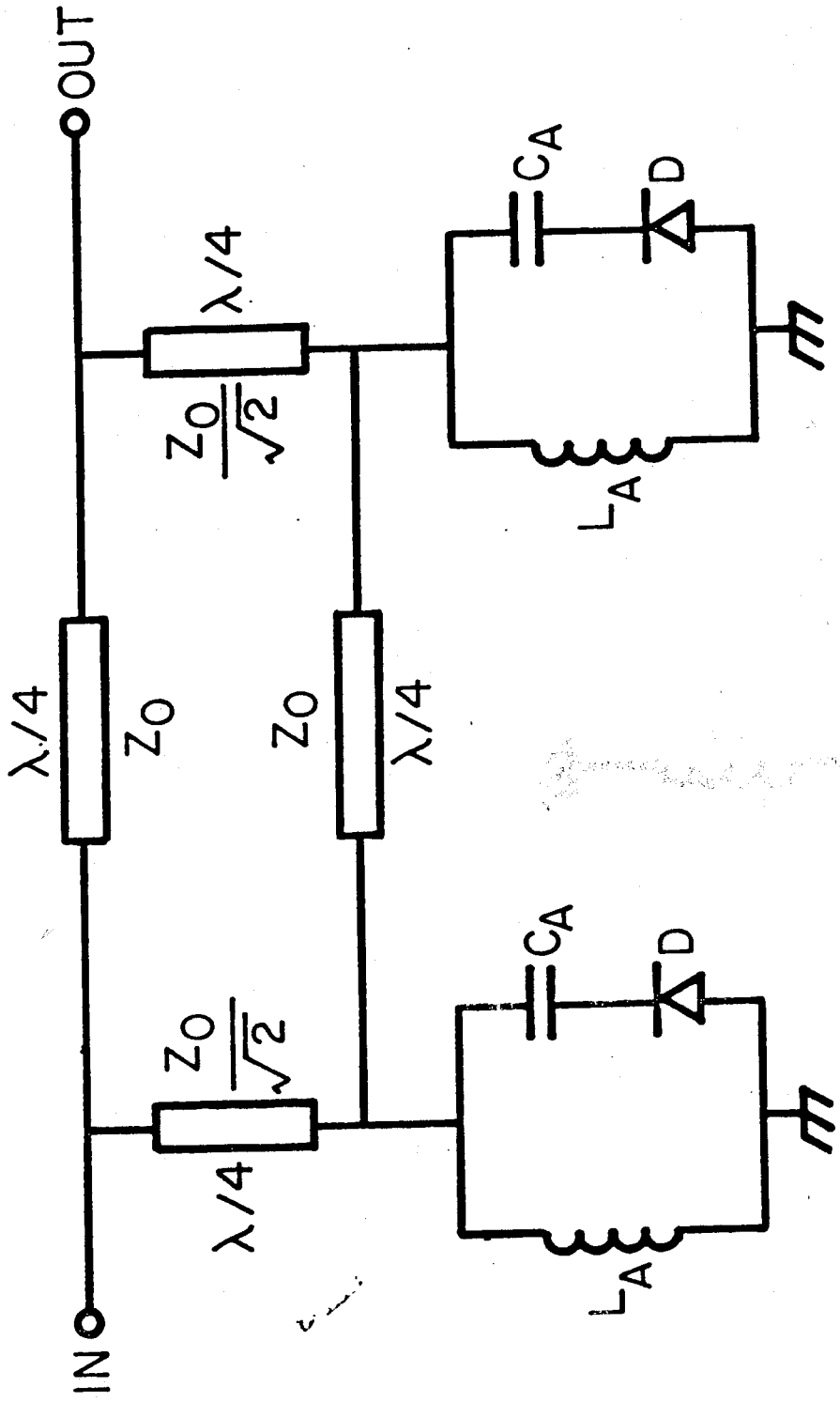
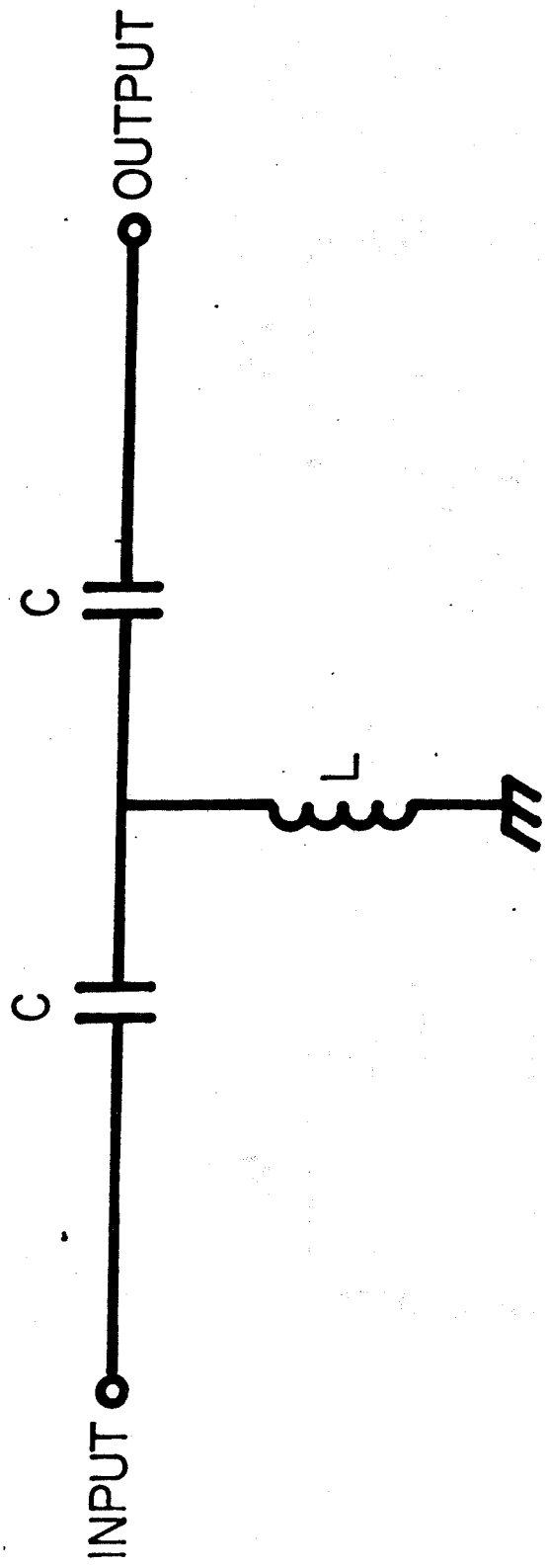


Figure 6b



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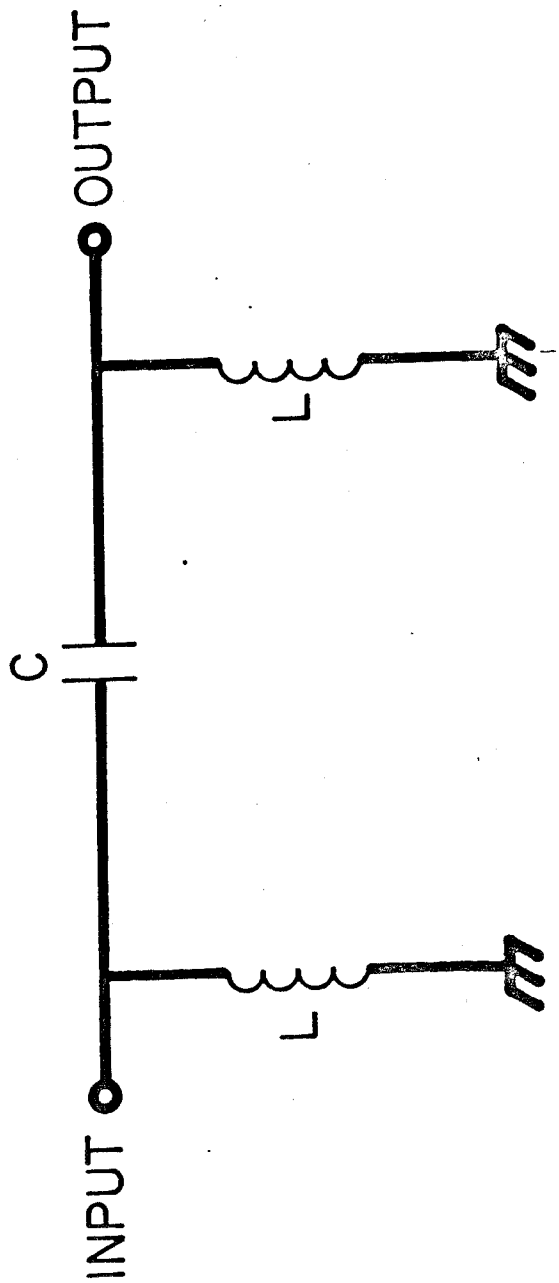

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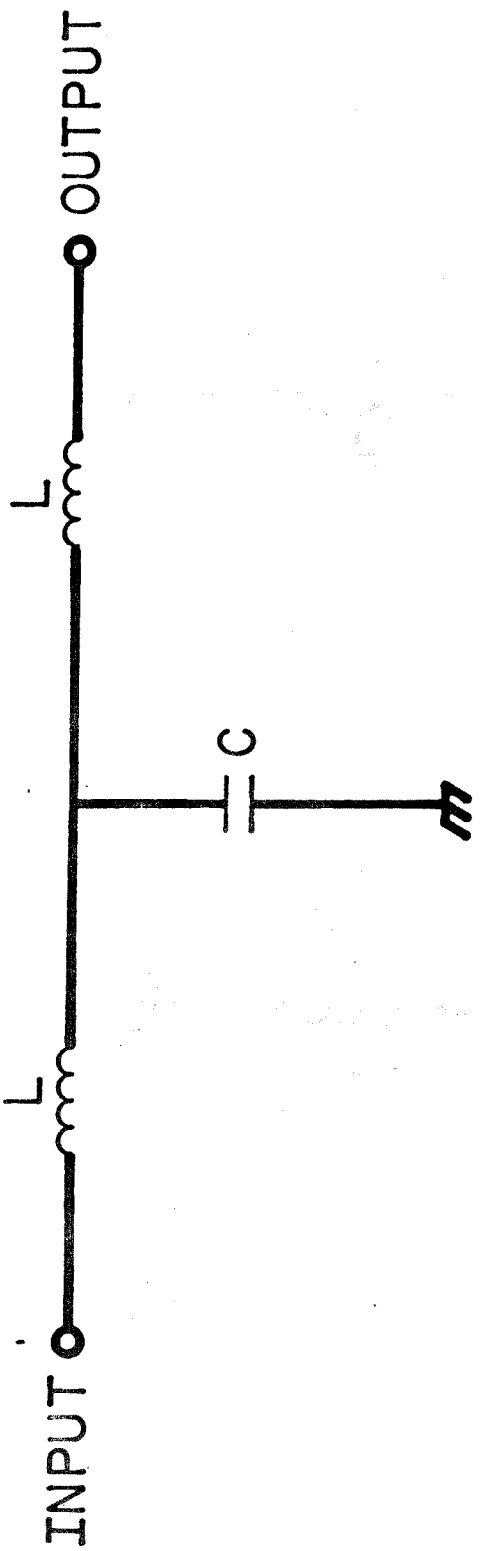

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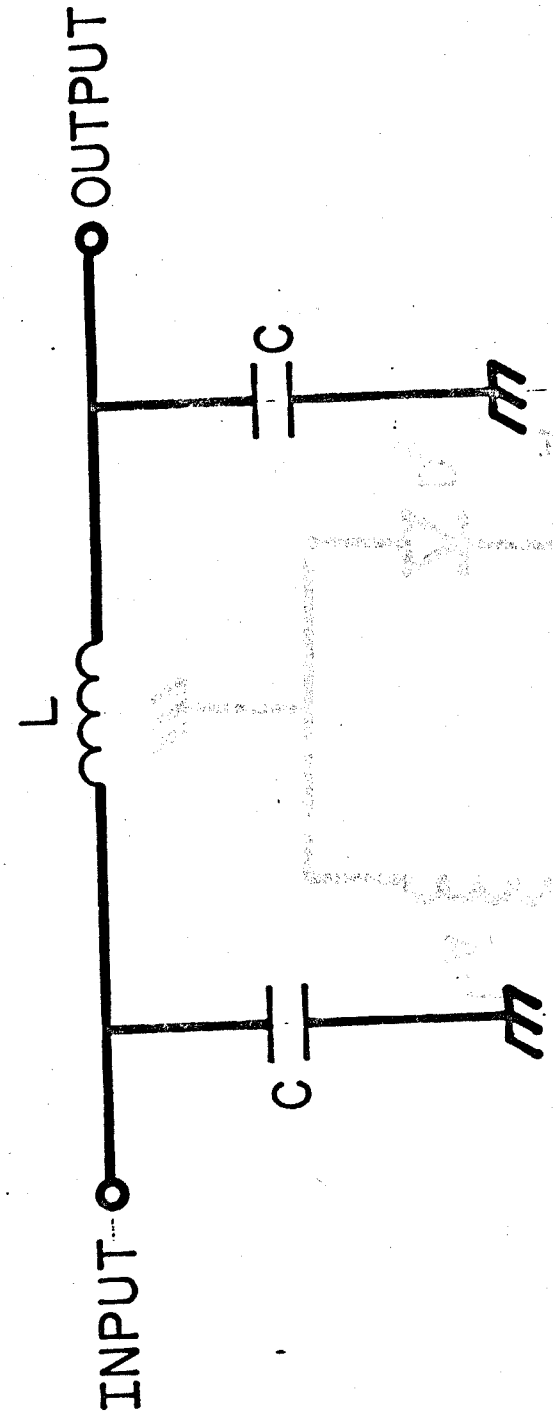

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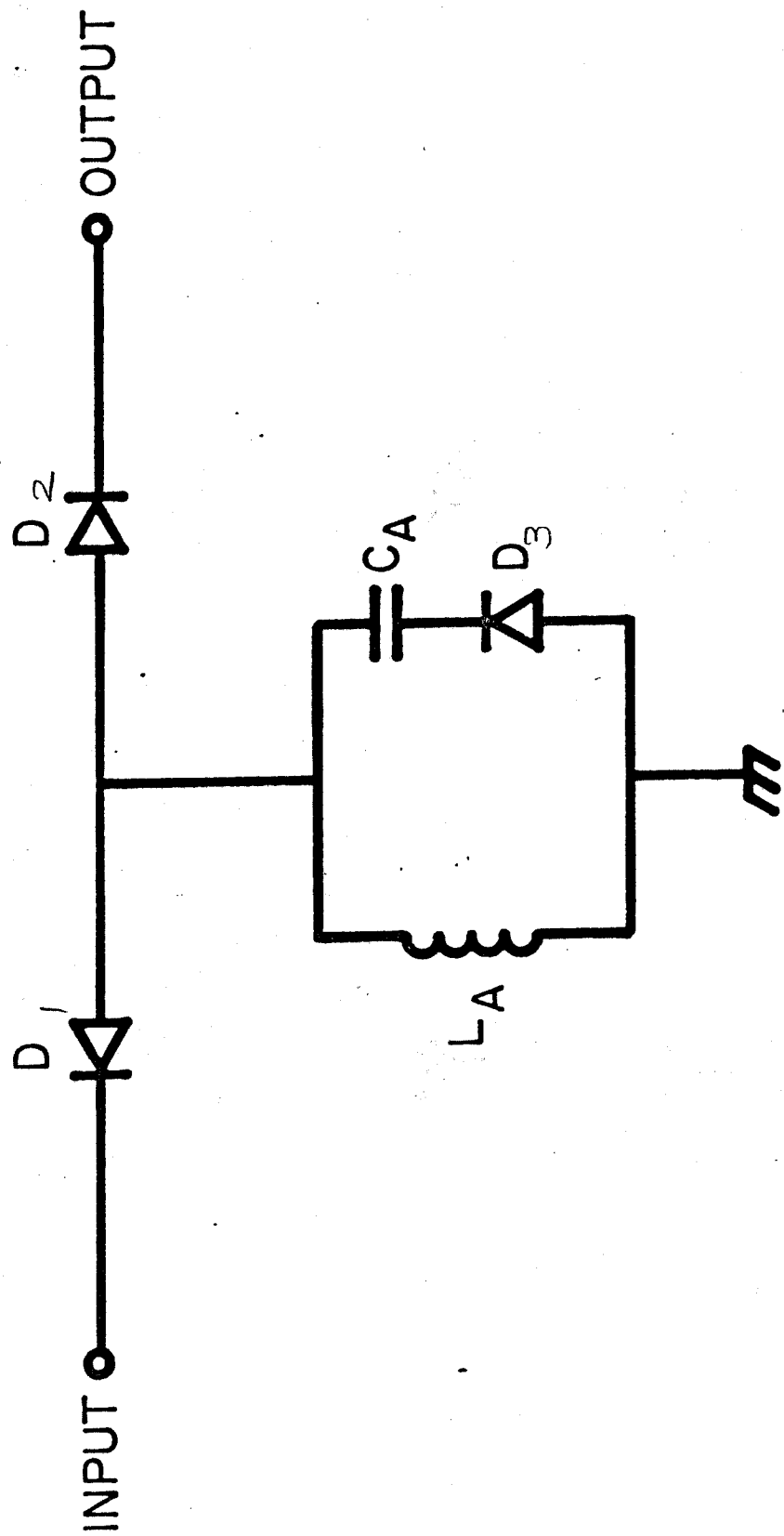
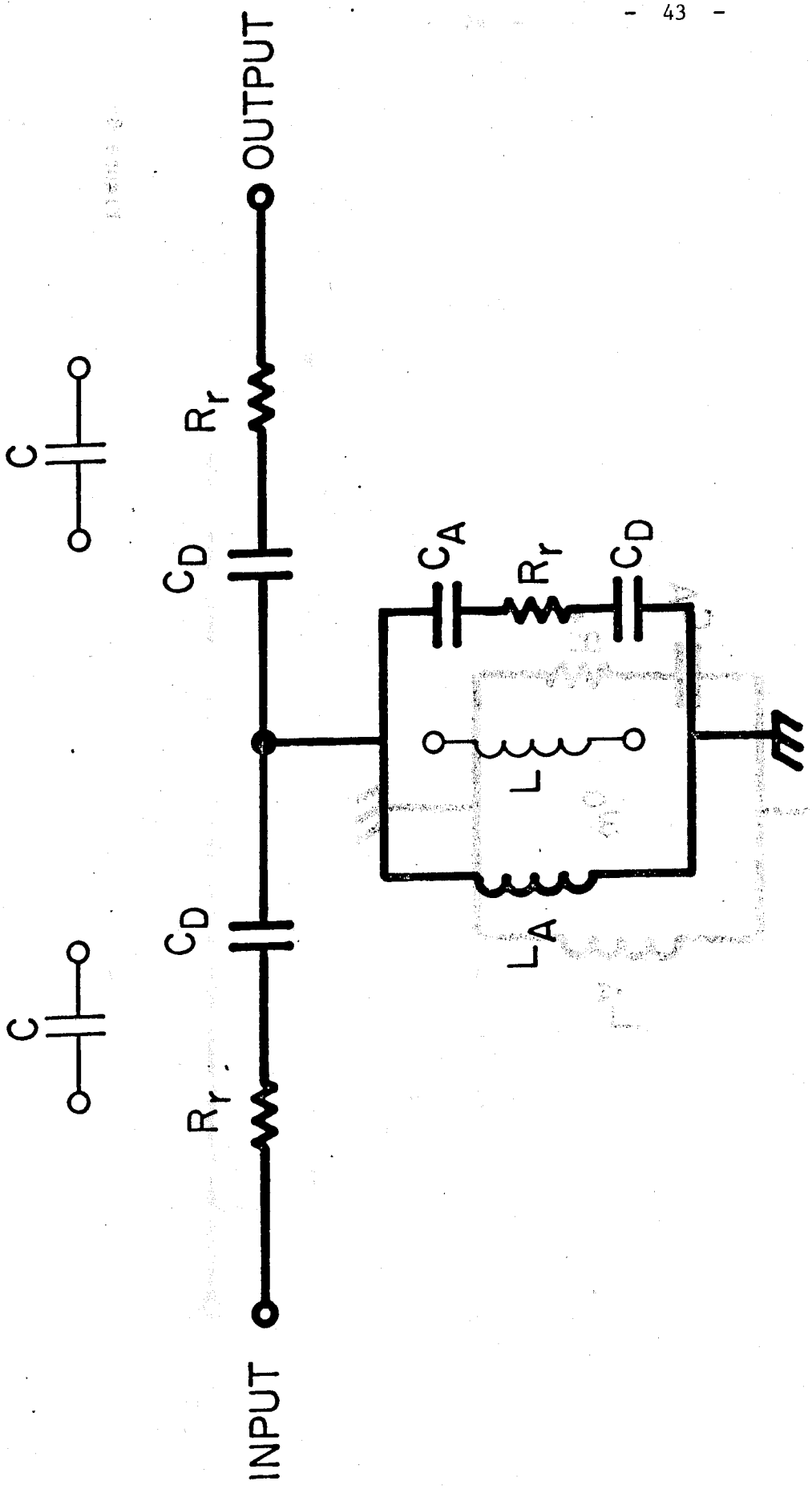


Figure 8a



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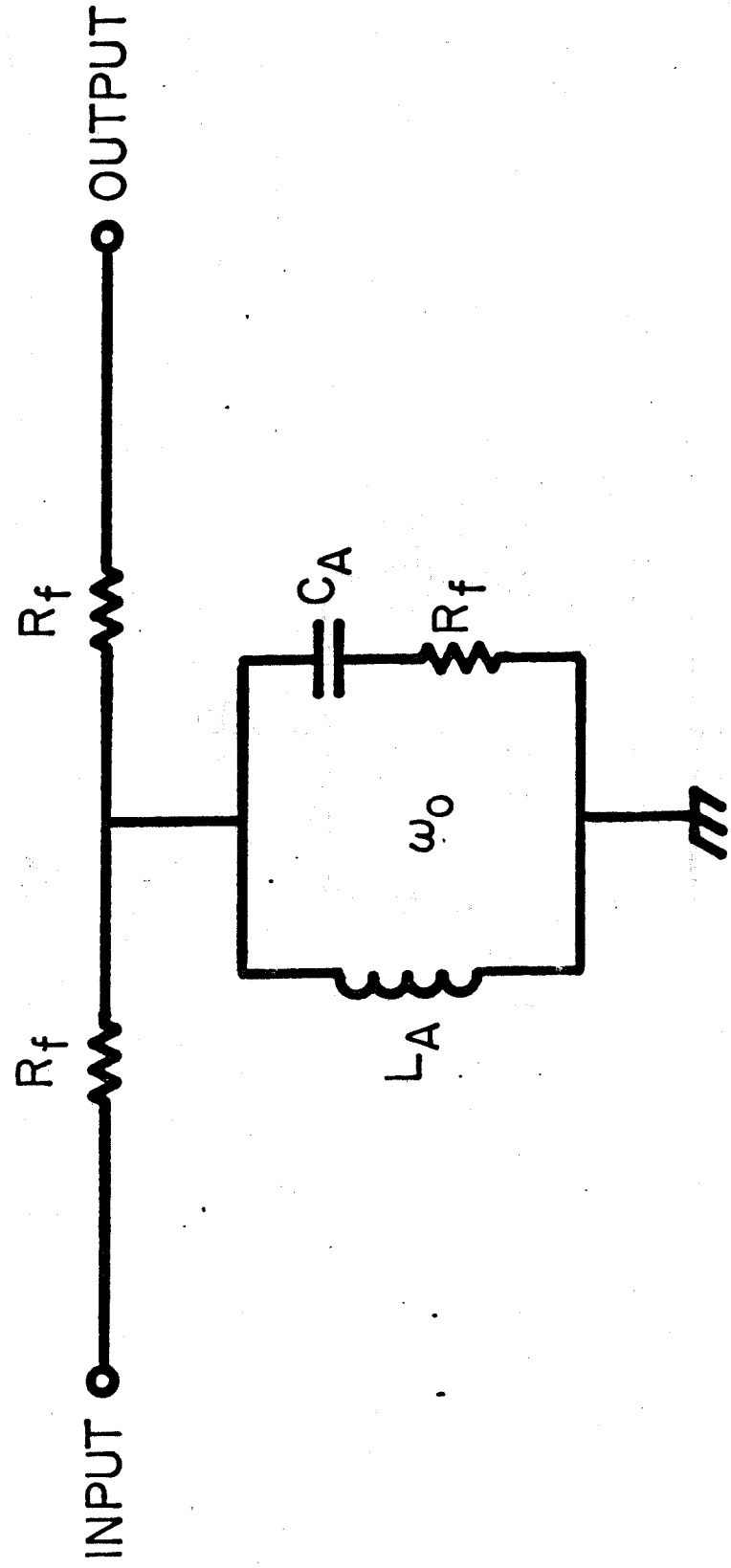

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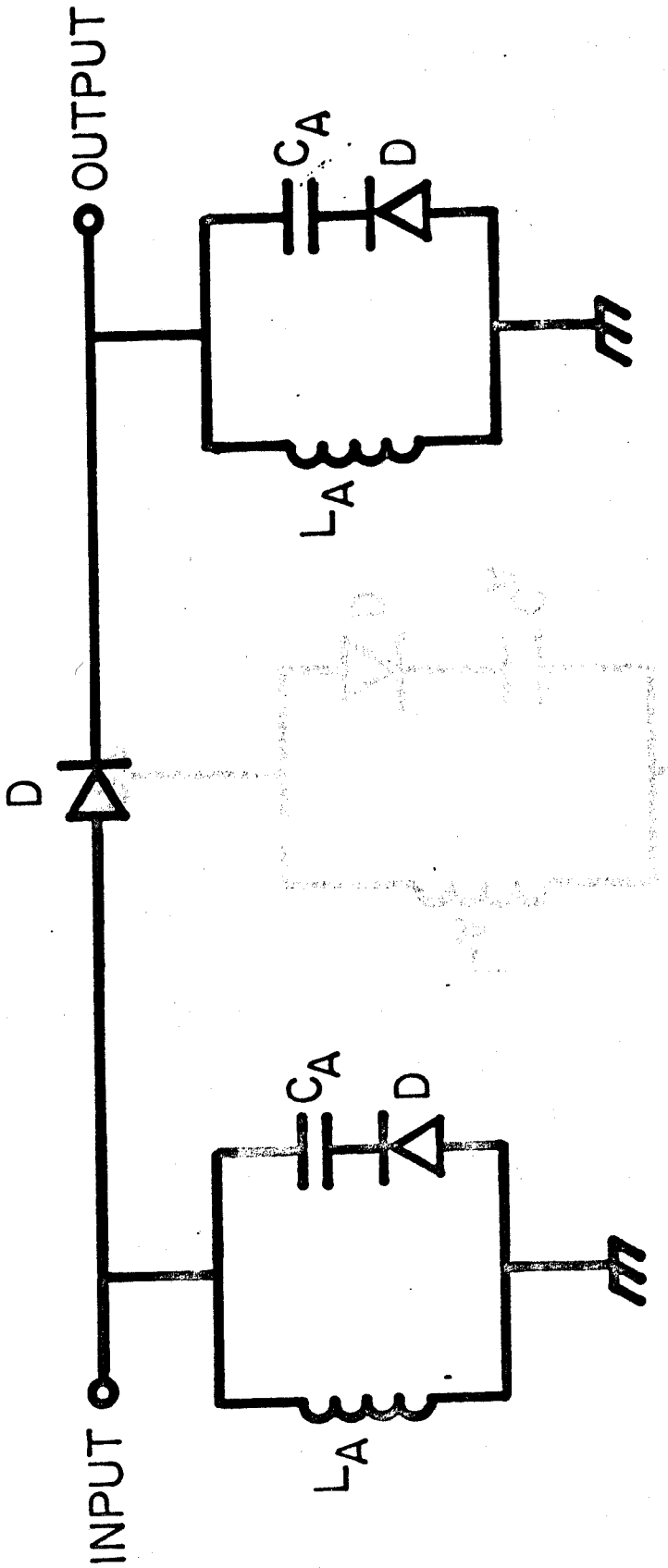

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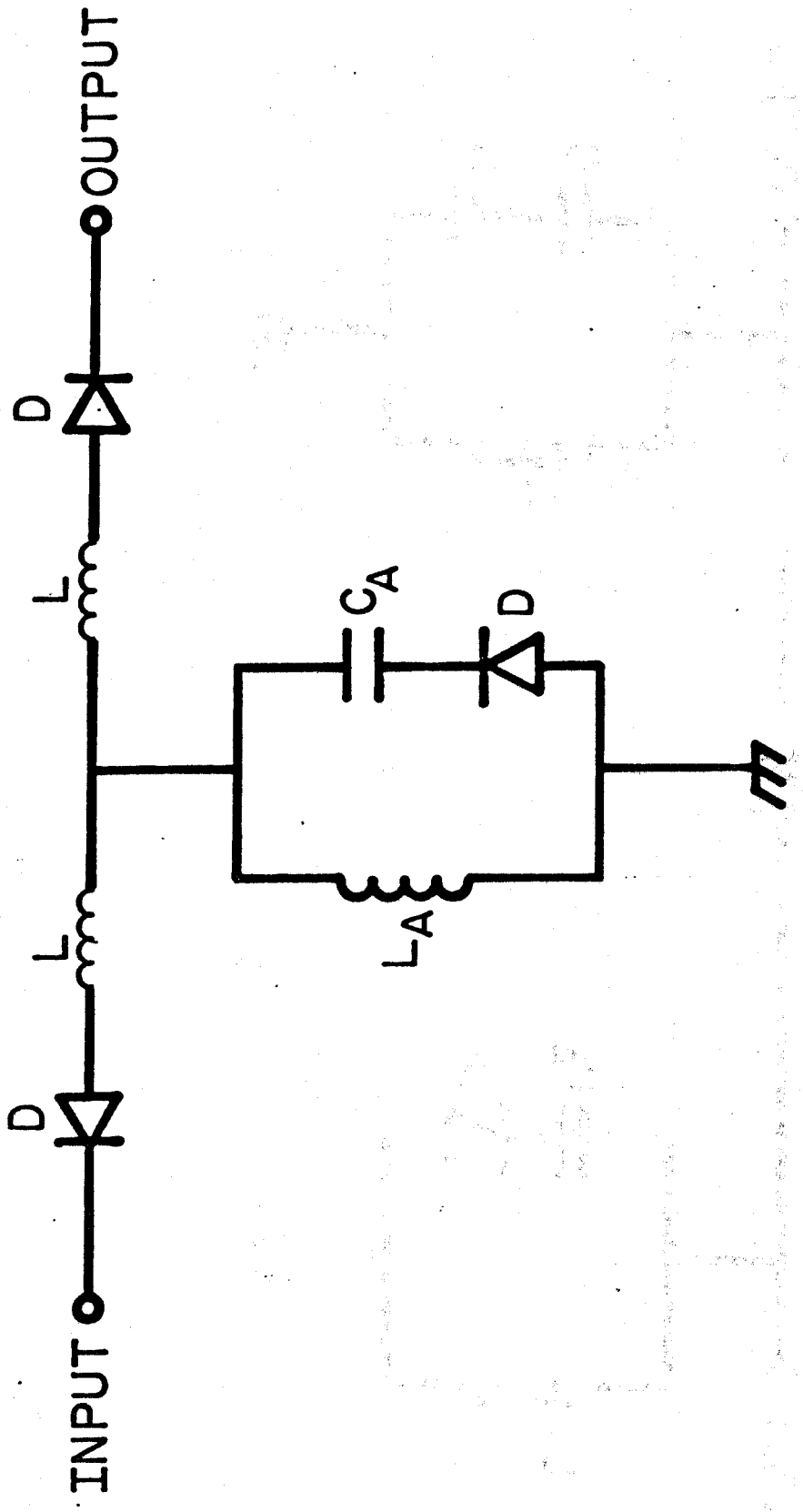
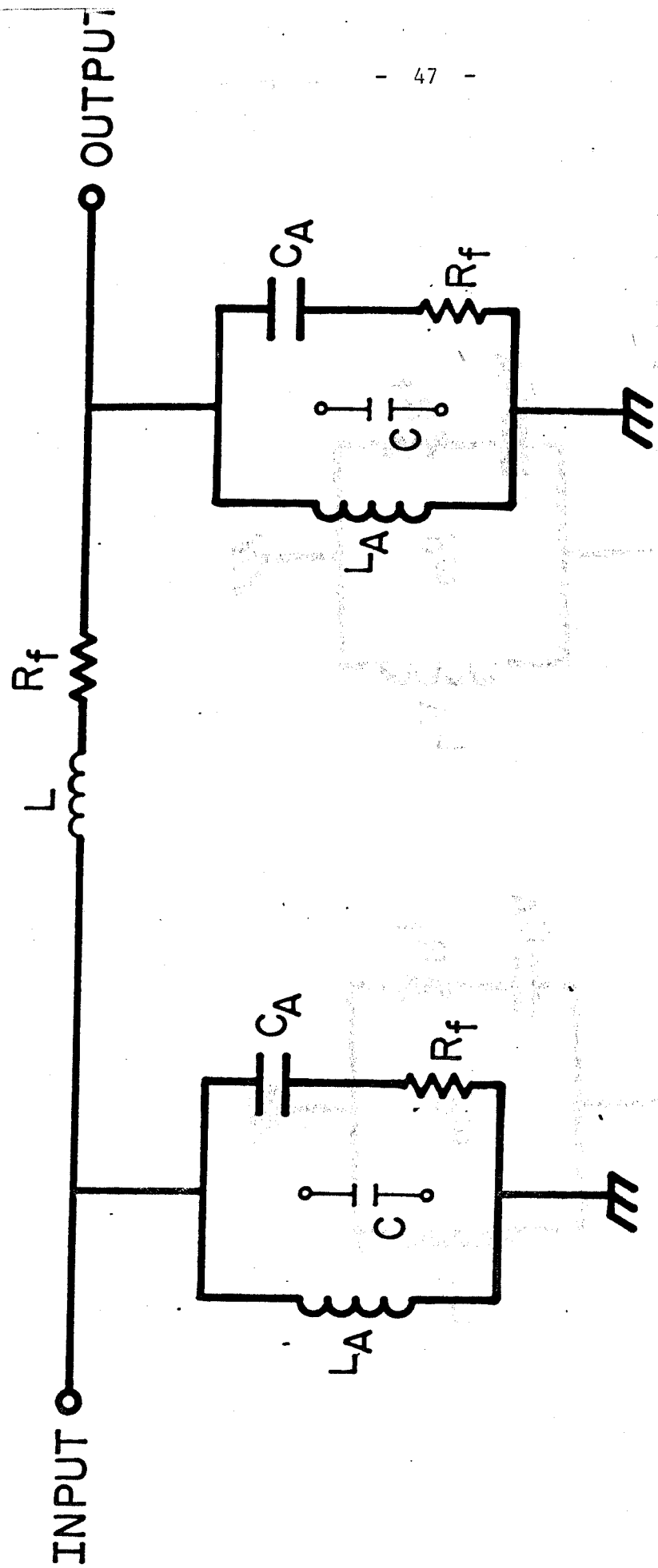


Figure 10a



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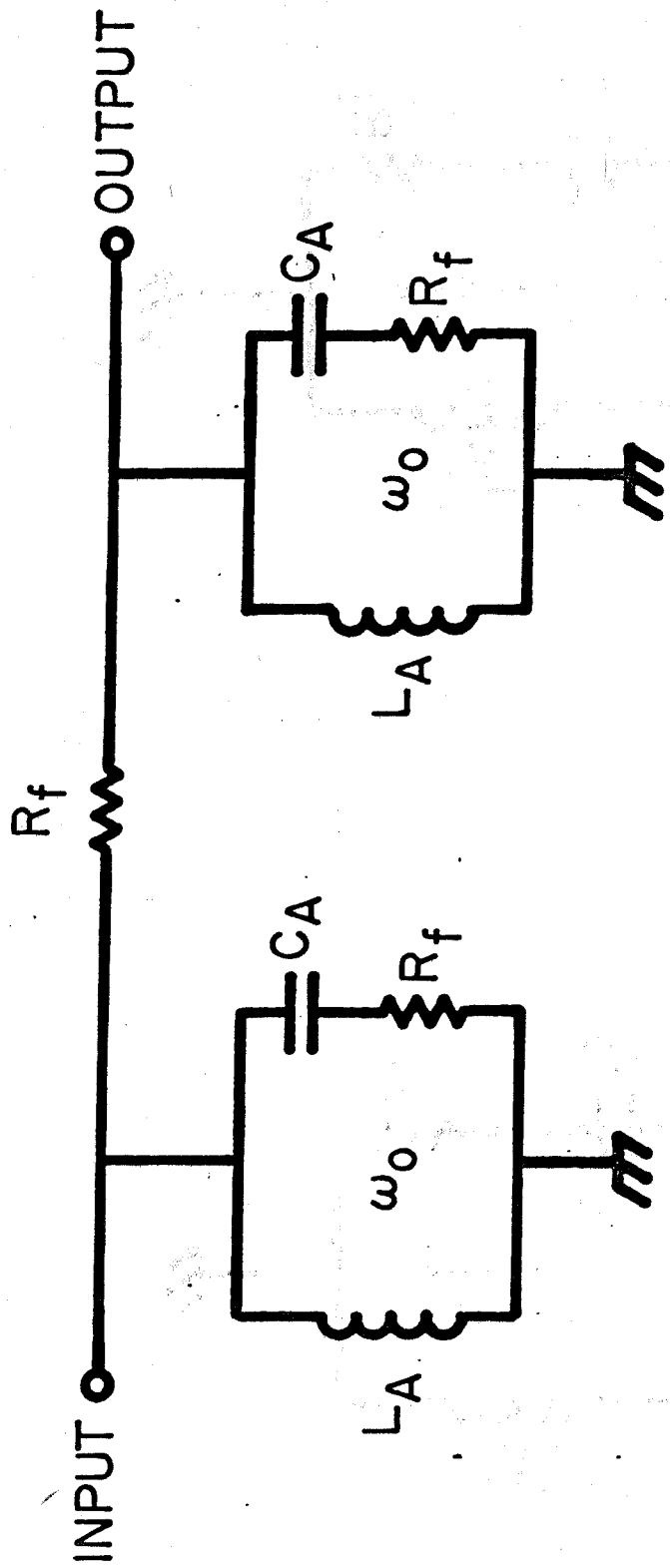

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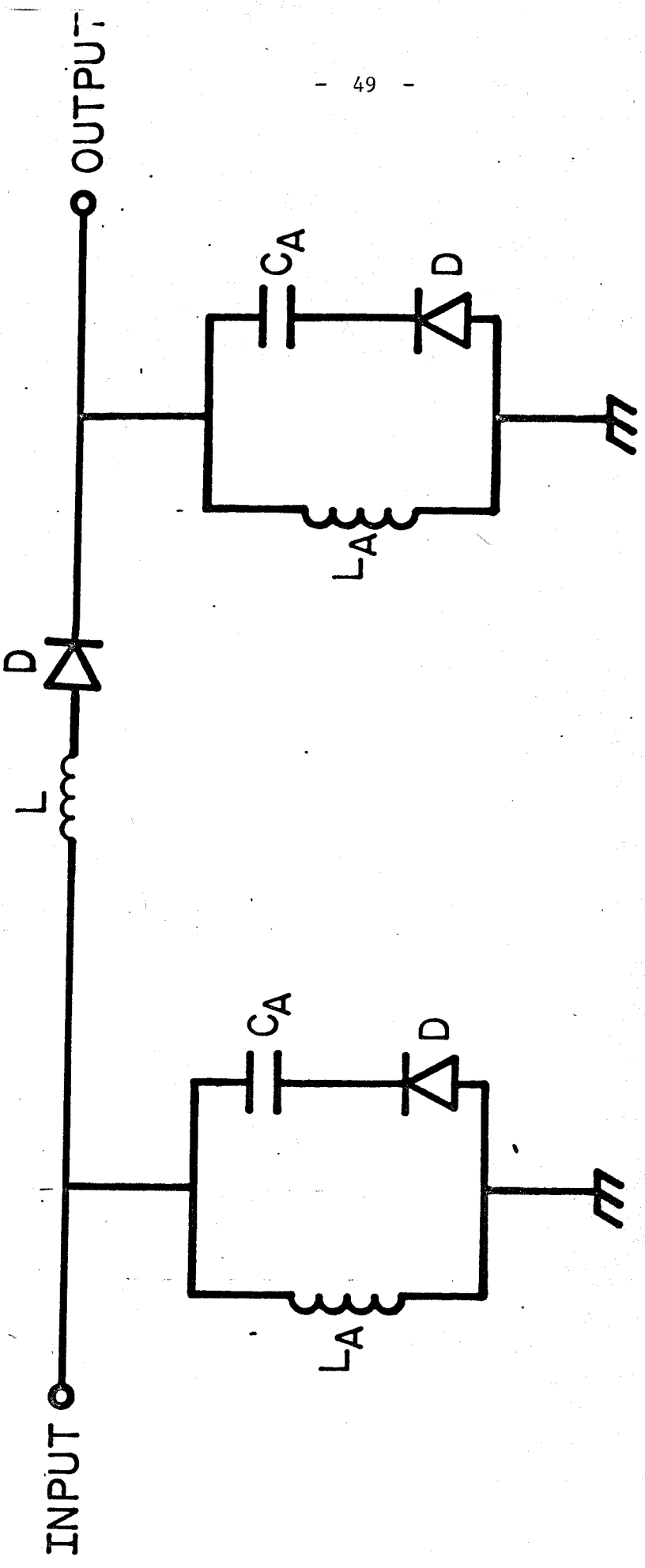

Figure 11